High-performance Embedded Artificial Intelligence System-on-Chip AI SoC Yulong810A (Datasheet rev. 1.30)

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1. OVERVIEW

Yulong810A is a new generation of embedded Artificial Intelligence (AI) series processor chip developed by ORBITA. The device provides high-end/high-performance front-end image processing, front-end signal processing, intelligent control and acceleration platform supporting deep learning and Neural Network (NN) algorithms.

Yulong810A integrates a heterogeneous multi-core architecture microprocessor (CPU + AI accelerator), manufactured with Fully Depleted - Silicon On Insulator (FD-SOI) semiconductor technology. The device provides high performance, high reliability and low power consumption characteristics oriented to aerospace, intelligent security, robotics, AIoT, intelligent manufacturing, intelligent transportation and many other applications.

The Yulong810A is based on :

- 4-core ARM Cortex-A9 processing unit and 4-core SPARC V8 processing unit, including main features such as integer processing unit (IU), floating point processing unit (FPU), high-speed first-level cache memory (L1 Cache), memory management unit (MMU), NEON coprocessor, and high-speed second-level cache memory (L2 Cache), etc.
- H.265/H.264/JPEG and JPEG2000 codecs suitable for high-performance video image processing, and a variety of on-chip peripherals, including including CameraLink, MIPI, BT1120, LVDS Display, RapidIO, PCIe, GigaEthernet, USB2.0, Nand Flash controller, SPI Nor Flash controller, SDIO, 1M/10M 1553B bus Controller, CAN bus controller, EMI controller, SPI master, I2C master, I2S controller, UART, timer, RTC, DMA, Watchdog, GPIO, PWM and other functional modules.
- Complete on-chip debugging system. For the ARM A9 core, users can connect to the CoreSight debug module through the JTAG interface in order to access the internal registers, memory, and on-chip peripherals for software and hardware debugging.

Yulong810A is supported by Orbita's Software Development Kit suitable to develop AI software programs quickly and efficiently. The device supports development frameworks such as Google TensorFlow and Caffe, and software libraries such as OPENCL\OPENVX\OPENCV, which can be used for AI development as well. Yulong810A supports eCOS, VxWorks, Linux and other real-time embedded operating systems; users can easily realize high-performance multi-core parallel processing design for embedded real-time control system.

2. DEVICE FEATURES

2.1. Features

Yulong810A generic characteristics:

- System-on-Chip based on 22 nm semiconductor FDX process, SEL immune technology;
- Packaged in FCBGA-896, 25 x 25mm, 0.8pitch;
- Power supply: Core 0.8V, Digital IO 1.8V/3.3V, Analog IO 1.8V/2.5V/3.3V, DDR IO 1.2V/1.35V/1.5V ;
- Operating temperature range: -40°C ～ +125°C;
- Typical power consumption: 5W;

Yulong810A features:

- 4-core ARM-Cortex A9 main processing unit;
- 4-core SPARC V8 main processing unit;
- 512KB ARM A9 processor L2Cache module;
- 512KB SPARC V8 processor L2Cache module;
- Universal Storage Cache: AI coprocessor cache;
- 8 processor Graphic Processing Unit (GPU);
- 8 Neural Network Accelerator units (NNA);
- Vision Front End & Scheduler: AI processor task allocation and command processing unit;
- 1MB on-chip SRAM for AI coprocessor;
- Clock & Reset module;
- PLL: Phase-Locked Loop module for clock signals generation;
- Real Time Clock (RTC) module;
- Watchdog module;
- 4-channel Timer module;
- Pulse Width Modulator (PWM) generator;
- DMA module comprising 3 groups of 8 channels;
- 12-bit precision SAR ADC;
- 128-byte programable eFuse controller;
- H.264/H.265/JPEG ;
- JPEG2000 ;
- BootROM module;
- External Memory Interface (EMI);
- DDR3L/LPDDR3/ DDR4 controller;
- Nand Flash controller;
- QSPI Nor Flash controller;
- Standard interfaces:
  - RapidIO;
  - PCIE, support PCIE Gen1, GEN2 protocols);
  - MIPI: MIPI CSI-2 controller;
  - BT1120;
  - LVDS video output controller, on-chip integrated LVDS TX PHY;
  - SDIO/eMMC controller, SD3.0 and eMMC v4.5;
  - Giga-Ethernet, external PHY supported;
  - Camera Link 2.0 ;
  - 2-channel USB 2.0 OTG ;
  - 1553B;
  - CAN;
  - 4-channel I^2C;
  - I^2S;
  - 2-channel SPI ; master/slave modes;
  - 4-channel UART;
  - 64 GPIO independently configurable.
- Voltage/Temperature sensors (VT sensors);

2.2. Simplified block diagram

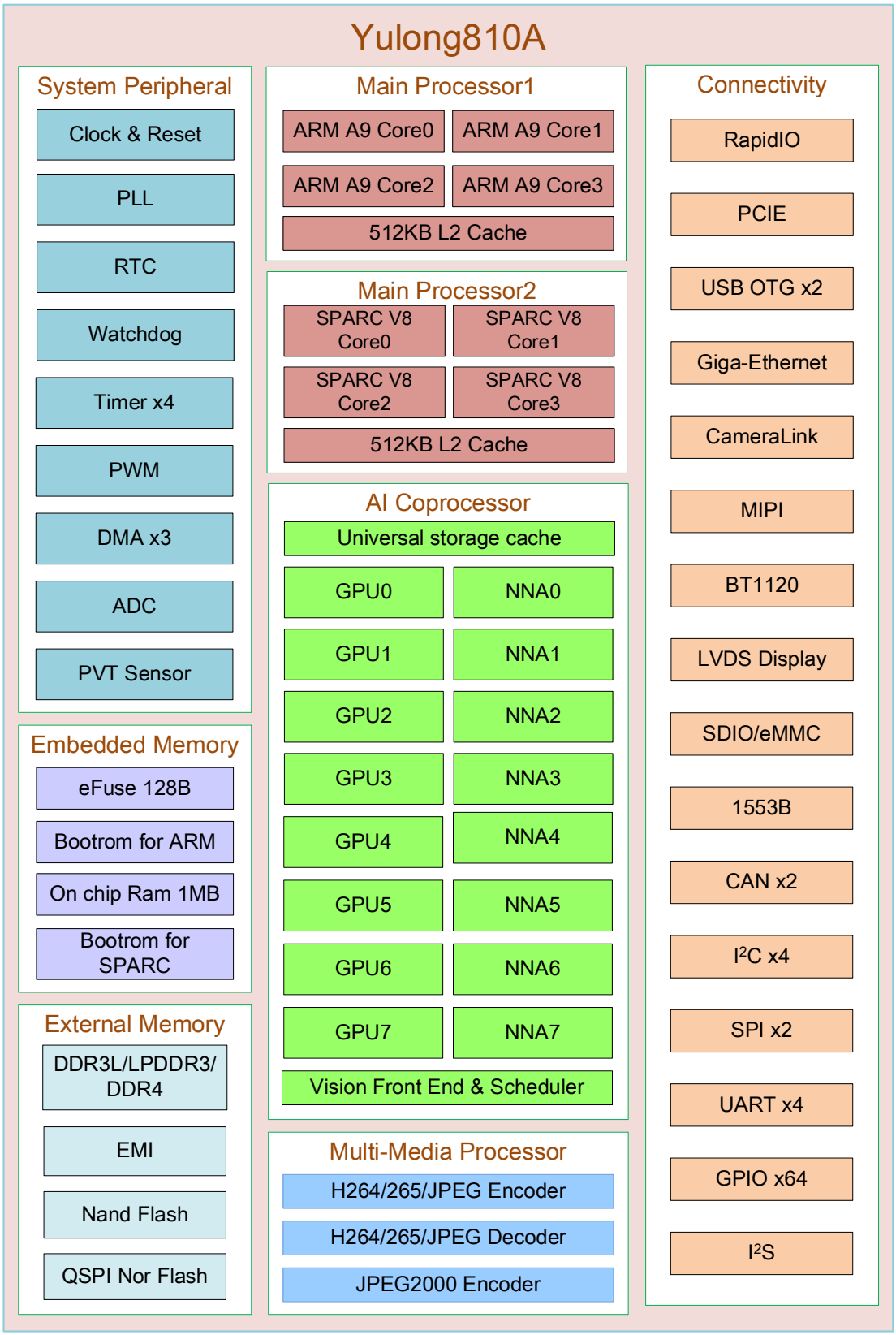

Figure 2-1 Simplified block diagram

3. SoC MODULES CHARACTERISTICS

3.1. Main processing core

- Main processor1
  - 4-core ARM CortexA9 processor -Working frequency range 1GHz@0.8V(Typical Case);
  - 32KB L1 Instruction Cache;
  - 32KB L1 Data Cache;
  - In-core timer and watchdog module;
  - 512KB L2 Cache;
  - Each core contains a superscalar variable length 8-stage pipeline, supports out-of-order execution, and has a dynamic branch prediction function;
  - Fully implement the ARM architecture v7-A instruction set;
  - NEON floating-point vector co-processing unit;
  - ARM NEON Advanced SIMD (Single Instruction, Multiple Data) for higher multimedia and signal processing;
  - Integrated PL310 L2 Cache;
  - Integrated CoreSight debugging unit, supports JTAG-based hardware breakpoint and multi-core debugging.
- Main processor2
  - 4-core SPARC V8 processor -Working frequency range 700MHz@0.8V(Typical Case);
  - 32KB L1 Instruction Cache;
  - 16KB L1 Data Cache;
  - 512KB L2 Cache;
  - Each core contains a superscalar variable length 7-stage pipeline;
  - Integrated DSU debugging unit, supports JTAG-based hardware breakpoint and multi-core debugging.

3.2. AI coprocessor

- GPU – Graphic processing Unit :
  - Use standard shader core instruction set;
  - 24 Enhanced Vision Instruction Sets (EVIS);
  - 16-bit/32-bit/64-bit floating-point operation;
  - 64GFLOPS peak computing capability.
- NNA – Neural Network Accelerator:
  - Matrix parallel convolution Multiplier Accumulator (MAC) unit ;
  - Compression and pruning of Neural Network multidimensional array processing;
  - 8-bit/16 bit fixed-point operation;
  - 12 TOPS peak computing performance;

3.3. Image coprocessing unit

- H.264/H.265/JPEG encoder :
  - Read/Write video data from Memory through the AXI4 interface;
  - HEVC encoding performance 3840x2160@30fps (main10 level5.1);
  - H.264 encoding performance 3840x2160@30fps (high profile);
  - JPEG encoding performance 3840x2160@30fps;
  - Output format YCbCr 4:2:0;
  - Support sampling bit depth 8bpc;
  - Support image down sampling;
  - Support slice/frame type: I, P, B three.

- H.264/H.265/JPEG decoder:
  - Read/Write video data from Memory through the AXI4 interface;
  - HEVC decoding performance 3840x2160@30fps (main10 level5.1);
  - H.264 decoding performance 3840x2160@30fps (high level5.2);
  - JPEG decoding performance 3840x2160@30fps;
  - Support 1 post processing (1 post processing) output;
  - Support OpenMax IL API;
  - Support Libva and Libdrm;
  - Support embedded reference frame compression.

- JPEG2000 Encoder :
  - JPEG2000 PART 1 lossy or lossless compression;
  - Advanced bit rate control engine;
  - Supported sampling format:
    - Grayscale sampling -Double elements: 4:4, 4:2, 4:1, and 4:0;
    - Three elements: 4:4:4, 4:2:2, 4:1:1, and 4:2:0;
    - Four elements: 4:4:4:4, 4:2:2:2, 4:1:1:1, and 4:2:0:0;
  - 8bit sampling accuracy per element;
  - up to 65535 x 65535 image resolution;
  - 4096 x 2160 slice accuracy;
  - Single/multi- quality layer coding;
  - Error recovery coding;
  - Support standard compatible code stream (JPC) or file (JP2) output.

3.4. On-chip Memory/Storage

- RAM memory:

  SoC integrates 1024KB on-chip SRAM which can be accessed by all master devices on the chip and can be used as a high-bandwidth cache.

- eFUSE:

SoC integrates 128Byte on-chip eFuse memory to be used for secured access to Cortex-A9.

- BootROM:
  Bootloader program is hardwired in the SoC chip.

3.5. External memory interface

DDR4/DDR3L/LPDDR3 controller:

- DDR4 up to 2666Mbps;
- LPDDR3 up to 1866Mbps;
- DDR3L up to 1600Mbps;
- single-rank mode;
- 3GB memory capacity;
- 64bit data width;
- 8bit ECC.

NAND FLASH controller

- 4 Chip Select signals, supports 1 ~ 8 address cycles, no maximum capacity limit;
- 8/16 bit FLASH IO bus width;
- 512KB, 2KB, 4KB and 8KB page size, SLC/MLC NAND flash device;
- Supports standard Flash device commands; provides Up mode for Flash interface operation of special commands;
- dual plane operation;
- Automatic on-chip buffer error correction; the internal ECC circuit can correct up to 8 or 15-bit random errors in every 512B data, or up to 24 or 40 or 60-bit random errors in every 1024B data.
- DMA operation;
- Data protection mode.

External Memory Interface controller (EMI)

- 8bit and 16bit data width; can support 16-bit boot through EMI;
- 4 address Chip Select signals, each allocated with 32MB address space;
- CPU mode and DMA mode;
- Programmable asynchronous read and write time;
- Address/data multiplexing and page mode.

Quad Serial Peripheral Interface (QSPI) Nor Flash controller

- DMA transfer mode;
- Up to 50MHz rate;
- Four SPI operation modes;
- Full duplex mode;
- Programmable MSB or LSB;
- Up to 2 external slave devices.

SD/SDIO/MMC high speed memory card interfaces

- SD3.0 and eMMCv4.5 standard compliance;
- 4-bit SD and SDIO transmission, support the highest UHS-I SDR-104 mode (max. 104 MB/s);
- 4-bit or 8-bit MMC card transmission, support SDR and DDR mode up to 52MHz (max. 104 MB/s).

3.6. System components

Real Time Clock (RTC): alarm and timing function

- Supports year/day/hour/minute/second/millisecond timings;
- Time accuracy compensation;
- Timing value initialization;
- 1s time deviation per day at 25°C;
- Time alarm function.

Watchdog

- 16-bit counter;
- Interrupt generation and reset signals when the timeout occurs;
- Reset the chip when the system fails.

Timer

- 3 counting modes: free running, cycle counting, single counting;
- 4 independent 32bit down counters;
- 4 independent interrupt signals;
- 4 groups of input clock capture pins;

Direct Memory Access (DMA)

- 3 DMA controllers, each constituted by 8 channels;
- Distributed/gathered DMA based on Linked Lists;
- Transmission mode of address increment/decrement or no change.

3.7. Peripheral video interfaces

- Bit allocation;
- Data format: -Mono 8/10/12/14/16; -RAW 8/10/12/14/16; -RGB 24/30/36;
- Pixel mapping according to following standards:
  - VESA (Video Electronics Standards Association) ;
  - JEIDA (Japanese Electronic Industry Development Association) ;
- LVDS transmitter outputs the remapped parallel data;
- LVDS single channel output (4 lanes), the maximum parallel data width is 28 bit;
- Max. 150MHz pixel clock and LVDS clock;
- Typical resolutions:
  - VGA(640x480)@60fps ;
  - SVGA(800x600)@60fps ;
  - XGA(1024x768)@60fps ;
  - SXGA(1280x1024)@60fps ;
  - UXGA(1600x1200)@60fps ;
  - FHD(1920x1080)@60fps.

CameraLink

CameraLink data acquisition module is compliant with Camera Link v2.0 specification.

CameraLink module features:

- CameraLink lite/base/medium/full/ mode;
- Bit allocation;
- Data format: -Mono 8/10/12/14/16; -RAW 8/10/12/14/16; -RGB 24/30/36;
- Camera control signal:
  - CC1: pulse or static 0/1 signal;
  - CC2: pulse or static 0/1 signal;
  - CC3: pulse or static 0/1 signal;
  - CC4: pulse or static 0/1 signal.
- Communication signal: -
  - SerTFG: connect to UART RX;
  - SerTC: connect to UART TX;
- Communication baud rate support: 300bps to 1500Kbps;
- Pixel clock range: 20MHz to 297MHz.

MIPI CSI-2 serial interface

MIPI CSI-2 controller module integrates MIPI-D PHY and is used to receive the camera sensor data of the CSI-2 interface.

MIPI CSI-2 module features:

- MIPI standards compliance:
  - MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2)Version 1.2, January 2014 ;
  - MIPI Alliance Specification for D-PHY, Version 1.2, September 2014 ;
  - MIPI Alliance Specification for C-PHY, Version 1.0, October 2014;
- Up to 8 D-PHY RX data channels;
- Each D-PHY channel supports up to 2.5Gbps communication rate;

- Each C-PHY channel supports up to 2.5Gbps communication rate.

BT1120 HDTV digital video interface

BT1120 controller module is complaint with HDTV digital video interface standard BT1120.

3.8. High-speed serial interfaces

PCIe Gen2

The SoC includes a PCIe controller (built-in PHY) for PCI Express RC and EP applications.

PCIe controller features:

- 4 channels PCIe communication;
- Root complex operations and Endpoint operations;
- PCI Express Gen1 and Gen2 protocols;
- Gen2 (5.0 Gbps x 4 lanes);
- 128-bit internal data depth, 125MHz internal working frequency;
- ECRC generation and verification;
- RAS DES (Debug, Error injection, statistics);
- RAS DP (Data Protection) to verify data path and RAM;
- MSI (Message Signaled interrupt);
- Advanced power consumption and clock management (D3Cold and L1Sub not supported);
- Configurable BAR filter, I/O filter;
- Embedded DMA (4 read + 4 write channels);
- Built-in address conversion module;

Rapid IO Gen2

The chip includes a Rapid IO controller (built-in PHY).

PCIe controller features:

- 4-channel Rapid IO controller;
- Up to 5Gbps (BRC1) or 6.25Gbps (BRC2) rate;
- Compatible with RapidIO standard version 2.2;
- BRC1 supports 1.25Gbaud, 2.5Gbaud, 3.125Gbaud and 5Gbaud rate;
- BRC2 supports 6.25Gbaud rate;
- Up to 256 Byte data load;
- 34bit and 50bitRIO addressing;
- Message transmission: data and doorbell information;
- DMA mode to read and write.

10/100/1000 Mbps GMAC Gigabit Ethernet

GMAC controller features:

- GMII/RGMII interface;
- 10, 100 and 1000Mbps data transfer rate;
- Full duplex and half full duplex operation;
- Frame filtering operation;
- Hardware verification and error correction;

GMAC Gigabit Ethernet controller shall be used with off-chip Ethernet PHY

USB2.0

USB2.0 module features:

- 2 USB 2.0 On-The-Go (OTG) interfaces:
  - OTG2.0 supports master/slave functions and is fully compatible with the USB2.0
  - OTG1.3 supports non-OTG master mode
- Speed modes:
  - - High speed (HS, 480-Mbps);
  - Full speed (FS, 12-Mbps);
  - Low speed (LS, 1.5-Mbps);
- Up to 7 two-way endpoints, including control endpoint 0;
- Up to 14 main channels;
- SRP protocol and HNP protocol;
- Integrated internal DMA;

3.9. Low-speed peripheral interfaces

I²S;

I²S built-in sound module provides 24-bit stereo input/output.

I²S module features:

- 4-wire interface (WS, SCLK, SD_IN, SD_OUT)
- Supports standard I2S protocol; Master mode only;
- Transmission with a maximum of 24 bits data width

UART

The 4 UART interfaces module features:

- 4 UART interfaces;
- 2-wire standard;
- Flow control;
- 16-bit bus transceiver;
- Programmable frame length, parity check and stop bit length;
- Configurable Baud rate.

SPI

SPI module supports FIFO data, master/slave device controller, clock generation and synchronization logic

operation.

SPI module features:

- 2 identical SPI (SPI0-SPI1) interfaces;
- Master/Slave modes;
- Up to 50MHz transmission rate.

I²C

I²C module supports FIFO data, master/slave device controller, clock generation and synchronization logic operations

I²C module features:

- 4 identical I²C (I2C0 to I2C3) interfaces;
- Master/Slave modes;
- Up to 3.4Mbps:
- Operating modes: standard mode, fast mode and high-speed mode;
- 7-bit or 10-bit addressing.

GPIO interface

GPIO module features:

- Contains 64 independent configurable GPIO[63:0];
- Each signal is controlled by the corresponding bit of the data register and data direction register;
- GPIO[31:0] supports external interrupt; interrupt supports 4 trigger modes: rising edge, falling edge, high level and low level.

SAR ADC

The SoC integrates a Successive-Approximation Register Analog-to-Digital Converter (SAR ADC).

SAR ADC module features:

- 12-bit SAR ADC;
- 1MSPS low-speed mode or 5MSPS high-speed mode;
- DNL: +/-1.5 LSB, INL: +/-3 LSB;
- Analog input range: VREFH to VREFL;
- 8-channel single-ended or differential analog input.

1553B avionic bus:

1553B module features:

- Fully compliant with MIL-STD-1553B protocol/standard;
- Support BC, RT and BM working modes;
- 1Mbps and 10Mbps configurable data rate;

- supports data transmission rate is 1Mbps and 10Mbps configurable.
- Memory layout and Register settings compliant with BU-61580 standard.

CAN:

CAN bus module features:

- 2 CAN bus controllers;
- Two independent channels;
- Compliant with CAN 2.0B protocol;
- Support PeliCAN and BasicCAN two modes; these two modes can be selected through the clock divider register. The mapping of registers is different in BasicCAN and PeliCAN modes.

3.10. Power management and control

- Integrated on-chip power management unit;
- Integrated temperature sensor;
- Support multiple system power consumption modes;
- Integrated flexible gated clock design;

3.11. PVT sensor

The SoC integrate sensor measuring/monitoring chip Voltage and Temperature (VT);

3.12. Software support

- Heterogeneous multi-core (API) interfaces: OPENCL, OPENVX, OPENCV;
- Operating system (EOS): Linux, FreeRTOS;
- Device drivers and routines;

4. PACKAGE CHARACTERISTICS

4.1. Package mechanical outlines: FCBGA-896 / 0.8mm ball pitch

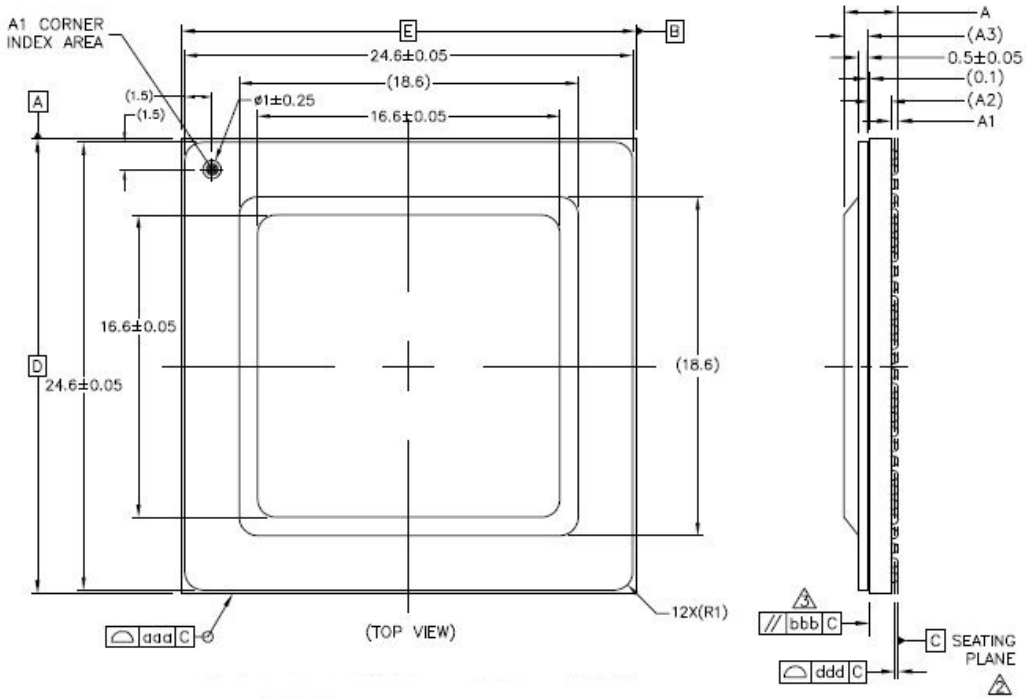

Figure 4-1 FCBGA896

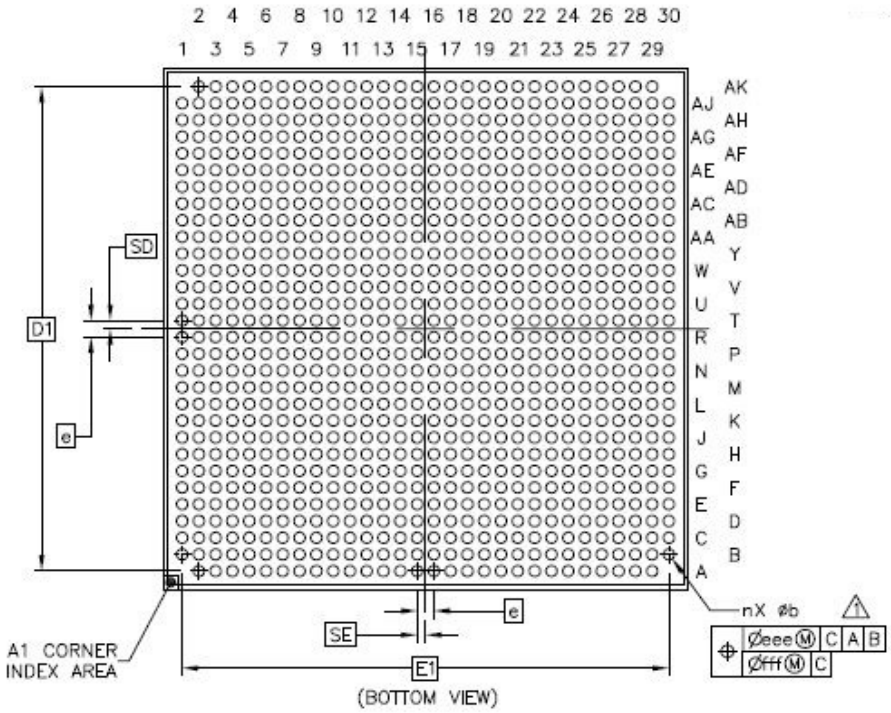

Figure 4-2 Ball allocation

Table 4-1 Package mechanical outline

Reference	Min. (mm)	Typical (mm)	Max. (mm)
A			3.18
A1	0.36		0.46
A2		1.17	REF
A3		1.30	REF
D		25.00	BSC
E		25.00	BSC
b	0.44	—	0.64
e		0.80	BSC
n		896 balls	
D1		23.20	BSC
E1		23.20	BSC
SD		0.40	BSC
SE		0.40	BSC
aaa		0.15	
bbb		0.25	
ddd		0.20	
eee		0.25	
fff		0.10	

4.2. FCBGA-896 Ball assignment

Yulong810A is packaged in FCBGA-896 Ball Grid Array package; with 0.8mm ball pitch.

4.2.1. Command, control and operation signals assignment

Table 4-2 Package mechanical outline

Category (num)	Ball allocation	Pin Name and Multiplexing	Function Description	I/O	Level
Global (5)	D26	TEST_MODE	Test mode – Active High	I	
	F25	BOOT_SEL0	0: A9 active, 1: A9 inactive	I	
	E24	BOOT_SEL1	0: SPARC active, 1: SPARC inactive	I	
	D25	BOOT_SEL2	0: ROM boot, 1: EMI boot	I	
	D24	RESETN	Chip reset, active low	I	
UART-0 (2)	F24	UART0_RXD*	UART0 receiver	I/O	
		I2C3_SCL	I2C 3 clock		
		2ND_GPIO33	Group 2 GPIO33		
	F23	UART0_TXD*	UART0 transmitter	I/O	
		I2C3_SDA	I^2C 3 data		
		2ND_GPIO34	Group 2 GPIO34		
UART-1 (2)	E23	UART1_RXD*	UART1 receiver	I/O	
		CAN1_RXD	CAN1 receiver		
		2ND_GPIO35	Group 2 GPIO35		
	D23	UART1_TXD*	UART1 transmitter	I/O	
		CAN1_TXD	CAN1 transmitter		
		2ND_GPIO36	Group 2 GPIO36		
UART-2 (2)	E22	UART2_RXD*	UART2 receiver	I/O	
		SPI1_SCLK	SPI1 clock		
		2ND_GPIO37	Group 2 GPIO37		
	D22	UART2_TXD*	UART2 transmitter	I/O	
		SPI1_CSN0	SPI1 Chip Select		
		2ND_GPIO38	Group 2 GPIO38		
UART-3 (2)	F22	UART3_RXD*	UART3 receiver	I/O	
		SPI1_MISO	SPI1 Master In/Slave Out		
		2ND_GPIO39	Group 2 GPIO39		
	F21	UART3_TXD*	UART3 transmitter	I/O	

		SPI1_MOSI	SPI1 Master Out/Slave In		
		2ND_GPIO40	Group 2 GPIO40		
I2C-0 (2)	A12	I2C0_SCL*	I²C0 clock	I/O	
		2ND_GPIO41	Group 2 GPIO41		
		TIMER_IN0	Timer 0 input		
	A13	I2C0_SDA*	I²C0 data	I/O	
		2ND_GPIO42	Group 2 GPIO42		
		TIMER_IN1	Timer 1 input		
I2C-1 (2)	A11	I2C1_SCL*	I²C1 clock	I/O	
		UART0_CTSn	UART0 transmitter enable		
		TRACECLK	A9 trace port clk signal		
	B11	I2C1_SDA*	I²C1 data	I/O	
		UART0_RTSn	UART transmitter request		
		TRACECTL	A9 trace port ctl signal		
SPI-0 (4)	D20	SPI0_SCLK*	SPI0 clock	I/O	
		2ND_GPIO43	Group 2 GPIO43		
	D21	SPI0_CSN*	SPI0 Chip Select	I/O	
		2ND_GPIO44	Group 2 GPIO44		
	E20	SPI0_MISO*	SPI0 Master In/Slave Out	I/O	
		2ND_GPIO45	Group 2 GPIO45		
	F19	SPI0_MOSI*	SPI0 Master Out/Slave In	I/O	
		2ND_GPIO46	Group 2 GPIO46		
QXHW (11)	F20	QXHW_CLK*	1553B clock	I/O	
		2ND_GPIO47	Group 2 GPIO47		
	E19	QXHW_RXA*	1553B bus A receiver	I/O	
		2ND_GPIO48	Group 2 GPIO48		
	D19	QXHW_RXA_N*	1553B bus A receiver	I/O	
		2ND_GPIO49	Group 2 GPIO49		
	E18	QXHW_RXB*	1553B bus B receiver	I/O	
		2ND_GPIO50	Group 2 GPIO50		
	D18	QXHW_RXB_N*	1553B bus B receiver	I/O	
		2ND_GPIO51	Group 2 GPIO51		
	F18	QXHW_TXA*	1553B bus A transmitter	I/O	
		2ND_GPIO52	Group 2 GPIO52		
	E17	QXHW_TXA_N*	1553B bus A transmitter	I/O	

		2ND_GPIO53	Group 2 GPIO53		
	D17	QXHW_TXA_INH*	1553B bus A transmitter inhibit	I/O	
		2ND_GPIO54	Group 2 GPIO54		
	E16	QXHW_TXB*	1553B bus B transmitter	I/O	
		2ND_GPIO55	Group 2 GPIO55		
	D16	QXHW_TXB_N*	1553B bus B transmitter	I/O	
		2ND_GPIO56	Group 2 GPIO56		
	F16	QXHW_TXB_INH*	1553B bus B transmitter inhibit	I/O	
		2ND_GPIO57	Group 2 GPIO57		
QSPI (6)	E12	QSPI_SCLK*	QSPI clock	I/O	
		2ND_GPIO58	Group 2 GPIO58		
	F10	QSPI_CSN0*	QSPI Chip Select	I/O	
		2ND_GPIO59	Group 2 GPIO59		
	D12	QSPI_MOSI*	QSPI Master Out/Slave In signal	I/O	
		2ND_GPIO60	Group 2 GPIO60		
	F12	QSPI_MISO*	QSPI Master In/Slave Out signal	I/O	
		2ND_GPIO61	Group 2 GPIO61		
	D11	QSPI_WPN*	QSPI write protect	I/O	
		2ND_GPIO62	Group 2 GPIO62		
	E11	QSPI_HOLDN*	QSPI hold signal	I/O	
		2ND_GPIO63	Group 2 GPIO63		
I2S (4)	C15	I2S_SCLK*	I2S bit clock output	I/O	
		I2C2_SCL	I^2C2 clock		
	A15	I2S_LRCK*	I2S frame clock output	I/O	
		I2C2_SDA	I^2C2 data		
	B14	I2S_SDI*	I2S input signal	I/O	
		PWM_OUT0	PWM signal output0		
	A14	I2S_SDO*	I2S output signal	I/O	
		PWM_OUT1	PWM signal output1		
CAN0 (2)	B13	CAN0_RXD*	CAN0 bus receiver	I/O	
		NF_CE[2]	NAND FLASH Chip Select2		
		EMI_LBN			
	C13	CAN0_TXD*	CAN0 bus transmitter	O	
		NF_CE[3]	NAND FLASH Chip Select3		
		EMI_UBN			

GPIO (8)	E15	GPIO_PIN0*	Group 1 GPIO0	I/O	
		EXT_IRQ0	External interrupt 0		
		BOOT_2ND[0]	2nd Boot configuration 0x0: UART; 0x1: SD Card; 0x2: eMMC Card; 0x3: QSPI Nor Flash; 0x4: NAND FLASH; 0x5-0xFF: reserved;		
	D15	GPIO_PIN1*	Group 1 GPIO1	I/O	
		EXT_IRQ1	External interrupt 1		
		BOOT_2ND[1]	Reference BOOT_2ND[0]		
	C14	GPIO_PIN2*	Group 1 GPIO2	I/O	
		EXT_IRQ2	External interrupt 2		
		BOOT_2ND[2]	Reference BOOT_2ND[0]		
	D14	GPIO_PIN3*	Group 1 GPIO3	I/O	
		EXT_IRQ3	External interrupt 3		
		BOOT_2ND[3]	Reference BOOT_2ND[0]		
	E14	GPIO_PIN4*	Group 1 GPIO4	I/O	
		WDT_OUT	SoC Watchdog reset output signal		
		BOOT_2ND[4]	Reference BOOT_2ND[0]		
	F14	GPIO_PIN5*	Group 1 GPIO5	I/O	
		QSPI_CSN1	QSPI Chip Select1		
		BOOT_2ND[5]	Reference BOOT_2ND[0]		
	E13	GPIO_PIN6*	Group 1 GPIO60	I/O	
		SPI0_CSN1	SPI0 Chip Select1		
		BOOT_2ND[6]	Reference BOOT_2ND[0]		
	D13	GPIO_PIN7*	Group 1 GPIO7	I/O	
		SPI1_CSN1	SPI1 Chip Select1		
		BOOT_2ND[7]	Reference BOOT_2ND[0]		
NAND FLASH (16)	B10	NF_CEN0*	NAND FLASH Chip Select 0	I/O	
		GPIO_PIN8	Group 1 GPIO8		
		TRACE0	A9 trace signal0		
	C10	NF_CEN1*	NAND FLASH Chip Select 1	I/O	
		GPIO_PIN9	Group 1 GPIO9		
		TRACE1	A9 trace signal1		

	A10	NF_ALE*	NAND FLASH address latch enable	I/O	
		GPIO_PIN10	Group 1 GPIO10		
		TRACE2	A9 trace signal2		
	D10	NF_CLE*	NAND FLASH command latch enable	I/O	
		GPIO_PIN11	Group 1 GPIO11		
		TRACE3	A9 trace signal3		
	E10	NF_REN*	NAND FLASH read signal	I/O	
		GPIO_PIN12	Group 1 GPIO12		
		TRACE4	A9 trace signal4		
	C11	NF_WEN*	NAND FLASH write signal	I/O	
		GPIO_PIN13	Group 1 GPIO13		
		TRACE5	A9 trace signal5		
	A9	NF_WPN*	NAND FLASH write protect	I/O	
		GPIO_PIN14	Group 1 GPIO14		
		TRACE6	A9 trace 6		
	E9	NF_RBN*	NAND FLASH busy	I/O	
		GPIO_PIN15	Group 1 GPIO15		
		TRACE7	A9 trace 7		
	C9	NF_IO0*	NAND FLASH data 0	I/O	
		GPIO_PIN16	Group 1 GPIO16		
		TRACE8	A9 trace 8		
	D9	NF_IO1*	NAND FLASH data 1	I/O	
		GPIO_PIN17	Group 1 GPIO17		
		TRACE9	A9 trace 9		
	F8	NF_IO2*	NAND FLASH data 2	I/O	
		GPIO_PIN18	Group 1 GPIO18		
		TRACE10	A9 trace 10		
	F7	NF_IO3*	NAND FLASH data 3	I/O	
		GPIO_PIN19	Group 1 GPIO19		
		TRACE11	A9 trace 11		
	E8	NF_IO4*	NAND FLASH data 4	I/O	
		GPIO_PIN20	Group 1 GPIO20		
		TRACE12	A9 trace 12		
	D8	NF_IO5*	NAND FLASH data 5	I/O	
		GPIO_PIN21	Group 1 GPIO21		

		TRACE13	A9 trace 13		
	C8	NF_IO6*	NAND FLASH data 6	I/O	
		GPIO_PIN22	Group 1 GPIO22		
		TRACE14	A9 trace 14		
	B8	NF_IO7*	NAND FLASH data 7	I/O	
		GPIO_PIN23	Group 1 GPIO23		
		TRACE15	A9 trace 15		
USB-0	C12	USB0_VBUS_VLDEN*		O	
		SDIO_VOLT_EN			
EMI (51)	G2	EMI_CSN0*	EMI Chip Select0	I/O	
		GPIO_PIN24	Group 1 GPIO24		
	F5	EMI_CSN1*	EMI Chip Select1	I/O	
		GPIO_PIN25	Group 1 GPIO25		
	F2	EMI_CSN2*	EMI Chip Select2	I/O	
		GPIO_PIN26	Group 1 GPIO26		
	F1	EMI_CSN3*	EMI Chip Select3	I/O	
		GPIO_PIN27	Group 1 GPIO27		
	G4	EMI_OEN*	EMI output enable	I/O	
		GPIO_PIN28	Group 1 GPIO28		
	G3	EMI_WEN*	EMI write enable	I/O	
		GPIO_PIN29	Group 1 GPIO29		
	H6	EMI_WAIT0*		I/O	
		GPIO_PIN30	Group 1 GPIO30		
	H5	EMI_WAIT1*		I/O	
		GPIO_PIN31	Group 1 GPIO31		
	G6	EMI_WAIT2*		I/O	
		GPIO_PIN32	Group 1 GPIO32		
	G5	EMI_WAIT3*		I/O	
		GPIO_PIN33	Group 1 GPIO33		
	G1	EMI_DQ0*	EMI data0	I/O	
		GPIO_PIN34	Group 1 GPIO34		
	H1	EMI_DQ1*	EMI data1	I/O	
		GPIO_PIN35	Group 1 GPIO35		
	H2	EMI_DQ2*	EMI data2	I/O	
		GPIO_PIN36	Group 1 GPIO36		

	H3	EMI_DQ3*	EMI data3	I/O	
		GPIO_PIN37	Group 1 GPIO37		
	H4	EMI_DQ4*	EMI data4	I/O	
		GPIO_PIN38	Group 1 GPIO38		
	J6	EMI_DQ5*	EMI data5	I/O	
		GPIO_PIN39	Group 1 GPIO39		
	J5	EMI_DQ6*	EMI data6	I/O	
		GPIO_PIN40	Group 1 GPIO40		
	J2	EMI_DQ7*	EMI data7	I/O	
		GPIO_PIN41	Group 1 GPIO41		
	J1	EMI_DQ8*	EMI data8	I/O	
		NF_IO[8]	NAND FLASH data 8		
	K1	EMI_DQ9*	EMI data9	I/O	
		NF_IO[9]	NAND FLASH data 9		
	K2	EMI_DQ10*	EMI data10	I/O	
		NF_IO[10]	NAND FLASH data 10		
	K3	EMI_DQ11*	EMI data11	I/O	
		NF_IO[11]	NAND FLASH data 11		
	K4	EMI_DQ12*	EMI data12	I/O	
		NF_IO[12]	NAND FLASH data 12		
	K5	EMI_DQ13*	EMI data13	I/O	
		NF_IO[13]	NAND FLASH data 13		
	K6	EMI_DQ14*	EMI data14	I/O	
		NF_IO[14]	NAND FLASH data 14		
	L6	EMI_DQ15*	EMI data15	I/O	
		NF_IO[15]	NAND FLASH data 15		
	L5	EMI_A0*	EMI 0	I/O	
		GPIO_PIN42	Group 1 GPIO42		
		BT1120_CLK	BT1120 clock		
	L4	EMI_A1*	EMI 1	I/O	
		GPIO_PIN43	Group 1 GPIO43		
		BT1120_D15	BT1120 data15		
	L3	EMI_A2*	EMI 2	I/O	
		GPIO_PIN44	Group 1 GPIO44		
		BT1120_D14	BT1120 data14		

	L2	EMI_A3*	EMI 3	I/O	
		GPIO_PIN45	Group 1 GPIO45		
		BT1120_D13	BT1120 data13		
	M2	EMI_A4*	EMI 4	I/O	
		GPIO_PIN46	Group 1 GPIO46		
		BT1120_D12	BT1120 data12		
	M3	EMI_A5*	EMI 5	I/O	
		GPIO_PIN47	Group 1 GPIO47		
		BT1120_D11	BT1120 data11		
	M4	EMI_A6*	EMI6	I/O	
		GPIO_PIN48	Group 1 GPIO48		
		BT1120_D10	BT1120 data10		
	M5	EMI_A7*	EMI7	I/O	
		GPIO_PIN49	Group 1 GPIO49		
		BT1120_D9	BT1120 data9		
	M6	EMI_A8*	EMI8	I/O	
		GPIO_PIN50	Group 1 GPIO50		
		BT1120_D8	BT1120 data8		
	N5	EMI_A9*	EMI9	I/O	
		GPIO_PIN51	Group 1 GPIO51		
		BT1120_D7	BT1120 data7		
	N4	EMI_A10*	EMI10	I/O	
		GPIO_PIN52	Group 1 GPIO52		
		BT1120_D6	BT1120 data6		
	N3	EMI_A11*	EMI11	I/O	
		GPIO_PIN53	Group 1 GPIO53		
		BT1120_D5	BT1120 data5		
	P4	EMI_A12*	EMI12	I/O	
		GPIO_PIN54	Group 1 GPIO54		
		BT1120_D4	BT1120 data4		
	P5	EMI_A13*	EMI13	I/O	
		GPIO_PIN55	Group 1 GPIO55		
		BT1120_D3	BT1120 data3		
	P6	EMI_A14*	EMI14	I/O	
		GPIO_PIN56	Group 1 GPIO56		

		BT1120_D2	BT1120 data2		
	R5	EMI_A15*	EMI15	I/O	
		GPIO_PIN57	Group 1 GPIO57		
		BT1120_D1	BT1120 data1		
	R4	EMI_A16*	EMI16	I/O	
		GPIO_PIN58	Group 1 GPIO58		
		BT1120_D0	BT1120 data0		
	T4	EMI_A17*	EMI17	I/O	
		GPIO_PIN59	Group 1 GPIO59		
	T5	EMI_A18*	EMI18	I/O	
		GPIO_PIN60	Group 1 GPIO60		
	T6	EMI_A19*	EMI19	I/O	
		GPIO_PIN61	Group 1 GPIO61		
	V6	EMI_A20*	EMI20	I/O	
		GPIO_PIN62	Group 1 GPIO62		
		TIMER_IN2	Timer input2		
	U5	EMI_A21*	EMI21	I/O	
		GPIO_PIN63	Group 1 GPIO63		
		TIMER_IN3	Timer input3		
	U4	EMI_A22*	EMI22	I/O	
		2ND_GPIO32	Group 2 GPIO32		
		USB0_VBUSVLD			
	V4	EMI_A23*	EMI23	O	
		SEN_MCLK			
	V3	EMI_A24*	EMI24	O	
		I2S_MCLK	I2S master clock output		
		EMI_ADV			
ARM JTAG (5)	Y4	JTAG0_TCK	A9 JTAG clk signal	I	
	W5	JTAG0_TMS	A9 JTAG tms signal	I	
	W4	JTAG0_TDI	A9 JTAG tdi signal	I	
	V5	JTAG0_TDO	A9 JTAG tdo signal	O	
	AA4	JTAG0_TRSTN	A9 JTAG reset signal	I	
SPARC JTAG(5)	Y5	JTAG1_TCK	SPARC JTAG clk signal	I	
	AA6	JTAG1_TMS	SPARC JTAG tms signal	I	
	AA5	JTAG1_TDI	SPARC JTAG tdi signal	I	

	Y6	JTAG1_TDO	SPARC JTAG tdo signal	O	
	AB4	JTAG1_TRSTN	SPARC JTAG reset signal	I	
SPARC CONFIG (9)	AB6	SPARC_DSUACT	SPARC DSU activity status signal	O	
	AC5	SPARC_DSUBRE	SPARC DSU break signal input When the signal changes from 0 to 1, the processor will enter Debug mode; In general, it is necessary to keep the signal at 0.	I	
	AC6	SPARC_DSUEN	SPARC DSU enable, When the input is 1, it will enter Debug mode, and input 0, it will enter Normal mode.	I	
	AB5	SPARC_DSUTX	SPARC DSU transmitter	O	
	AC4	SPARC_DSURX	SPARC DSU receiver	I	
	AD4	SPARC_UARTTX	SPARC UART transmitter	O	
	AD3	SPARC_UARTRX	SPARC UART receiver	I	
	AE4	SPARC_ERRORN	SPARC internal processing error signal	O	
	AD6	SPARC_REMAP	0: ROM boot, 1: EMI boot	I	
OSC (2)	L1	XTAL24M_IN	Crystal oscillator clock input	I	
	M1	XTAL24M_OUT	Crystal oscillator clock output	O	
ENET (27)	AE6	ENET_MII_TXCLK	Ethernet MII transmitter clock	I	
	AE5	ENET_MDC	Ethernet Management Data Clock	O	
	AF4	ENET_MDIO	Ethernet Management Data Input/Output	I/O	
	AF5	ENET_RXCLK	Ethernet receiver clock	I	
	AG5	ENET_TXCLK	Ethernet transmitter clock	O	
	AG4	ENET_CRS	PHY CRS signal,	I	
	AF6	ENET_COL	PHYconflict signal, active high	I	
	AG6	ENET_RXER	PHY error receiver, active high	I	
	AG7	ENET_RXDV	PHY data receiver, active high	I	
	AE7	ENET_RXD0	Ethernet receiver data0	I	
	AF8	ENET_RXD1	Ethernet receiver data1	I	
	AE8	ENET_RXD2	Ethernet receiver data2	I	
	AH8	ENET_RXD3	Ethernet receiver data3	I	
	AG9	ENET_RXD4	Ethernet receiver data4	I	
	AG8	ENET_RXD5	Ethernet receiver data5	I	
	AE9	ENET_RXD6	Ethernet receiver data6	I	
	AF9	ENET_RXD7	Ethernet receiver data7	I	
	AG11	ENET_TXER	PHY error transmitter, active high	O	

	AE10	ENET_TXEN	PHY data transmitter, active high	O	
	AG10	ENET_TXD0	Ethernet transmitter data0	O	
	AF11	ENET_TXD1	Ethernet transmitter data1	O	
	AF12	ENET_TXD2	Ethernet transmitter data2	O	
	AE12	ENET_TXD3	Ethernet transmitter data3	O	
	AE11	ENET_TXD4	Ethernet transmitter data4	O	
	AF13	ENET_TXD5	Ethernet transmitter data5	O	
	AG13	ENET_TXD6	Ethernet transmitter data6	O	
	AG12	ENET_TXD7	Ethernet transmitter data7	O	
RTC (6)	B1	XTAL32K_IN	RTC 32K clock input	I	
	C1	XTAL32K_OUT	RTC 32K clock input	O	
	D1	RTC_RESETN	RTC reset	I	
	E1	RTC_BUTTON	SoC Power on / off request outside RTC		
	C2	SOC_ISO_EN	Power isolation control of external PMIC to SOC	I	
	D2	SOC_PMIC_EN	Power on request of PMC output by SOC	O	
SDIO (14)	A6	SDIO_CCLK_OUT	SDIO clock output	O	
	C7	SDIO_CCMD	SDIO command output, active high	O	
	C5	SDIO_CDATA0	SDIO data0	I/O	
	D5	SDIO_CDATA1	SDIO data1	I/O	
	F6	SDIO_CDATA2	SDIO data2	I/O	
	E6	SDIO_CDATA3	SDIO data3	I/O	
	D6	SDIO_CDATA4	SDIO data4	I/O	
	C6	SDIO_CDATA5	SDIO data5	I/O	
	D7	SDIO_CDATA6	SDIO data6	I/O	
	E7	SDIO_CDATA7	SDIO data7	I/O	
	B6	SDIO_DATA_STROBE	SDIO data strobe signal	I	
	A7	SDIO_RESET_N*	Device reset signal output	O	
	A8	SDIO_CARD_DETECT_N	Card detection signal, active low	I	
	B7	SDIO_WRITE_PROTECT	Write protect signal, active low	I	
MIPI CSI2 (11)	AK11	MIPI_CK_N	MIPI clockN		
	AJ11	MIPI_CK_P	MIPI differential clockP		
	AK9	MIPI_D0_N	MIPI differential data0N		
	AJ9	MIPI_D0_P	MIPI differential data0P		

	AK10	MIPI_D1_N	MIPI differential data1N		
	AJ10	MIPI_D1_P	MIPI differential data1P		
	AK12	MIPI_D2_N	MIPI differential data2N		
	AJ12	MIPI_D2_P	MIPI differential data2P		
	AK13	MIPI_D3_N	MIPI differential data3N		
	AJ13	MIPI_D3_P	MIPI differential data3P		
	AH9	MIPI_REXT			
Camera Link (43)	AK19	CMLINK_RX_X0_N	Cameralink X-axis differential data input 0N	I	
	AJ19	CMLINK_RX_X0_P	Cameralink X-axis differential data input 0P	I	
	AK18	CMLINK_RX_X1_N	Cameralink X-axis differential data input 1N	I	
	AJ18	CMLINK_RX_X1_P	Cameralink X-axis differential data input 1P	I	
	AK16	CMLINK_RX_XCLK_N	Cameralink X-axis differential clock input N	I	
	AJ16	CMLINK_RX_XCLK_P	Cameralink X-axis differential clock input P	I	
	AK17	CMLINK_RX_X2_N	Cameralink X-axis differential data input 2N	I	
	AJ17	CMLINK_RX_X2_P	Cameralink X-axis differential data input 2P	I	
	AK15	CMLINK_RX_X3_N	Cameralink X-axis differential data input 3N	I	
	AJ15	CMLINK_RX_X3_P	Cameralink X-axis differential data input 3P	I	
	AF18	CMLINK_SerTC_OUT_P	Cameralink differential serial communication output P	O	
	AG18	CMLINK_SerTC_OUT_N	Cameralink differential serial communication output N	O	
	AG19	CMLINK_SerTFG_INM	Cameralink differential serial communication input M	I	
	AF19	CMLINK_SerTFG_INP	Cameralink differential serial communication input P	I	
	AE15	CMLINK_RTUNE			
	AG17	CMLINK_CC1_OUT_N	Cameralink control differential output 1N	O	
	AF17	CMLINK_CC1_OUT_P	Cameralink control differential output 1P	O	
	AG16	CMLINK_CC2_OUT_N	Cameralink control differential output	O	

			2N		
	AF16	CMLINK_CC2_OUT_P	Cameralink control differential output 2P	O	
	AG15	CMLINK_CC3_OUT_N	Cameralink control differential output 3N	O	
	AF15	CMLINK_CC3_OUT_P	Cameralink control differential output 3P	O	
	AG14	CMLINK_CC4_OUT_N	Cameralink control differential output 4N	O	
	AF14	CMLINK_CC4_OUT_P	Cameralink control differential output 4P	O	
	AG25	CMLINK_RX_Y0_N	Cameralink Y-axis differential data input 0N	I	
	AF25	CMLINK_RX_Y0_P	Cameralink Y-axis differential data input 0P	I	
	AG24	CMLINK_RX_Y1_N	Cameralink Y-axis differential data input 1N	I	
	AF24	CMLINK_RX_Y1_P	Cameralink Y-axis differential data input 1P	I	
	AG23	CMLINK_RX_YCLK_N	Cameralink Y-axis differential clock input N	I	
	AF23	CMLINK_RX_YCLK_P	Cameralink Y-axis differential clock input P	I	
	AG22	CMLINK_RX_Y2_N	Cameralink Y-axis differential data input 2N	I	
	AF22	CMLINK_RX_Y2_P	Cameralink Y-axis differential data input 2P	I	
	AG21	CMLINK_RX_Y3_N	Cameralink Y-axis differential data input 3N	I	
	AF21	CMLINK_RX_Y3_P	Cameralink Y-axis differential data input 3P	I	
	AK25	CMLINK_RX_Z0_N	Cameralink Z-axis differential data input 0N	I	
	AJ25	CMLINK_RX_Z0_P	Cameralink Z-axis differential data input 0P	I	
	AK24	CMLINK_RX_Z1_N	Cameralink Z-axis differential data input 1N	I	
	AJ24	CMLINK_RX_Z1_P	Cameralink Z-axis differential data input 1P	I	
	AJ23	CMLINK_RX_ZCLK_N	Cameralink Z-axis differential clock input N	I	
	AK23	CMLINK_RX_ZCLK_P	Cameralink Z-axis differential clock input P	I	
	AK22	CMLINK_RX_Z2_N	Cameralink Z-axis differential data input 2N	I	

	AJ22	CMLINK_RX_Z2_P	Cameralink Z-axis differential data input 2P	I	
	AK21	CMLINK_RX_Z3_N	Cameralink Z-axis differential data input 3N	I	
	AJ21	CMLINK_RX_Z3_P	Cameralink Z-axis differential data input 3P	I	
USB-0 (5)	C4	USB0_ID	USB0 OTG ID detection signal		
	A3	USB0_VBUS	USB0 power supply, connect to 5V input	I	
	B4	USB0_DP	USB0 positive differential data		
	A4	USB0_DM	USB0 negative differential data		
	A5	USB0_REXT			
USB-1 (3)	B2	USB1_DP	USB1 positive differential data		
	A2	USB1_DM	USB1 negative differential data		
	C3	USB1_REXT			
PCIe (18)	AJ5	PCIE_REF_CLK_P	PCIE differential Reference clock input P	I	
	AK5	PCIE_REF_CLK_M	PCIE differential Reference clock input M	I	
	AE2	PCIE_TX0_P	PCIE differential data output 0P	O	
	AE1	PCIE_TX0_M	PCIE differential data output 0M	O	
	AJ3	PCIE_RX0_P	PCIE differential data input 0P	I	
	AK3	PCIE_RX0_M	PCIE differential data input 0M	I	
	AF2	PCIE_TX1_P	PCIE differential data output 1P	O	
	AF1	PCIE_TX1_M	PCIE differential data output 1M	O	
	AJ4	PCIE_RX1_P	PCIE differential data input 1P	I	
	AK4	PCIE_RX1_M	PCIE differential data input 2M	I	
	AG2	PCIE_TX2_P	PCIE differential data output 2P	O	
	AG1	PCIE_TX2_M	PCIE differential data output 2M	O	
	AJ6	PCIE_RX2_P	PCIE differential data input 2P	I	
	AK6	PCIE_RX2_M	PCIE differential data input 2M	I	
	AH2	PCIE_TX3_P	PCIE differential data output 3P	O	
	AH1	PCIE_TX3_M	PCIE differential data output 3M	O	
	AJ7	PCIE_RX3_P	PCIE differential data input 3P	I	
	AK7	PCIE_RX3_M	PCIE differential data input 3M	I	
RapidIO (19)	P2	SRIO_RX0_P	RapidIO differential data input 0P	I	
	P1	SRIO_RX0_M	RapidIO differential data input 0M	I	

	W2	SRIO_TX0_P	RapidIO differential data output 0P	O	
	W1	SRIO_TX0_M	RapidIO differential data output 0M	O	
	R2	SRIO_RX1_P	RapidIO differential data input 1P	I	
	R1	SRIO_RX1_M	RapidIO differential data input 1M	I	
	Y2	SRIO_TX1_P	RapidIO differential data output 1P	O	
	Y1	SRIO_TX1_M	RapidIO differential data output 1M	O	
	T2	SRIO_RX2_P	RapidIO differential data input 2P	I	
	T1	SRIO_RX2_M	RapidIO differential data input 2M	I	
	AB2	SRIO_TX2_P	RapidIO differential data output 2P	O	
	AB1	SRIO_TX2_M	RapidIO differential data output 2M	O	
	U2	SRIO_RX3_P	RapidIO differential data input 3P	I	
	U1	SRIO_RX3_M	RapidIO differential data input 3M	I	
	AC2	SRIO_TX3_P	RapidIO differential data output 3P	O	
	AC1	SRIO_TX3_M	RapidIO differential data output 3M	O	
	AA2	SRIO_REF_CLK_P	RapidIO differential Reference clock input P	I	
	AA1	SRIO_REF_CLK_M	RapidIO differential Reference clock input M	I	
	AE13	HISS_ATEST		I/O	
Display (20)	A26	LVDS_TX_TA0N	LVDS differential data bus output 0N	O	
	B26	LVDS_TX_TA0P	LVDS differential data bus output 0P	O	
	A25	LVDS_TX_TA1N	LVDS differential data bus output 1N	O	
	B25	LVDS_TX_TA1P	LVDS differential data bus output 1P	O	
	A23	LVDS_TX_TA2N	LVDS differential data bus output 2N	O	
	B23	LVDS_TX_TA2P	LVDS differential data bus output 2P	O	
	A22	LVDS_TX_TA3N	LVDS differential data bus output 3N	O	
	B22	LVDS_TX_TA3P	LVDS differential data bus output 3P	O	
	A24	LVDS_TX_TAACLKN	LVDS differential clock bus output AAN	O	
	B24	LVDS_TX_TAACLKP	LVDS differential clock bus output AAP	O	
	A19	LVDS_TX_TABCLKN	LVDS differential clock bus output ABN	O	
	B19	LVDS_TX_TABCLKP	LVDS differential clock bus output ABP	O	
	A21	LVDS_TX_TA4N	LVDS differential data bus output 4N	O	
	B21	LVDS_TX_TA4P	LVDS differential data bus output 4P	O	
	A20	LVDS_TX_TA5N	LVDS differential data bus output 5N	O	
	B20	LVDS_TX_TA5P	LVDS differential data bus output 5P	O	

	A18	LVDS_TX_TA6N	LVDS differential data bus output 6N	O	
	B18	LVDS_TX_TA6P	LVDS differential data bus output 6P	O	
	A17	LVDS_TX_TA7N	LVDS differential data bus output 7N	O	
	B17	LVDS_TX_TA7P	LVDS differential data bus output 7P	O	
	C22	LVDS_TX_RTUNE			
DDR (172)	A28	PAD_MEM_DATA[0]	DDR data signal 0	I/O	
	A29	PAD_MEM_DATA[1]	DDR data signal 1	I/O	
	G26	PAD_MEM_DATA[10]	DDR data signal 10	I/O	
	E27	PAD_MEM_DATA[11]	DDR data signal 11	I/O	
	G28	PAD_MEM_DATA[12]	DDR data signal 12	I/O	
	D27	PAD_MEM_DATA[13]	DDR data signal 13	I/O	
	D28	PAD_MEM_DATA[14]	DDR data signal 14	I/O	
	G27	PAD_MEM_DATA[15]	DDR data signal 15	I/O	
	H25	PAD_MEM_DATA[16]	DDR data signal 16	I/O	
	H27	PAD_MEM_DATA[17]	DDR data signal 17	I/O	
	H28	PAD_MEM_DATA[18]	DDR data signal 18	I/O	
	J25	PAD_MEM_DATA[19]	DDR data signal 19	I/O	
	B28	PAD_MEM_DATA[2]	DDR data signal 2	I/O	
	K25	PAD_MEM_DATA[20]	DDR data signal 20	I/O	
	K26	PAD_MEM_DATA[21]	DDR data signal 21	I/O	
	K28	PAD_MEM_DATA[22]	DDR data signal 22	I/O	
	K27	PAD_MEM_DATA[23]	DDR data signal 23	I/O	
	F29	PAD_MEM_DATA[24]	DDR data signal 24	I/O	
	G29	PAD_MEM_DATA[25]	DDR data signal 25	I/O	
	G30	PAD_MEM_DATA[26]	DDR data signal 26	I/O	
	J29	PAD_MEM_DATA[27]	DDR data signal 27	I/O	
	K30	PAD_MEM_DATA[28]	DDR data signal 28	I/O	
	K29	PAD_MEM_DATA[29]	DDR data signal 29	I/O	
	C29	PAD_MEM_DATA[3]	DDR data signal 3	I/O	
	M30	PAD_MEM_DATA[30]	DDR data signal 30	I/O	
	M29	PAD_MEM_DATA[31]	DDR data signal 31	I/O	
	W29	PAD_MEM_DATA[32]	DDR data signal 32	I/O	
	V30	PAD_MEM_DATA[33]	DDR data signal 33	I/O	
	U30	PAD_MEM_DATA[34]	DDR data signal 34	I/O	
	V29	PAD_MEM_DATA[35]	DDR data signal 35	I/O	

	T29	PAD_MEM_DATA[36]	DDR data signal 36	I/O	
	P30	PAD_MEM_DATA[37]	DDR data signal 37	I/O	
	N30	PAD_MEM_DATA[38]	DDR data signal 38	I/O	
	N29	PAD_MEM_DATA[39]	DDR data signal 39	I/O	
	D29	PAD_MEM_DATA[4]	DDR data signal 4	I/O	
	AD28	PAD_MEM_DATA[40]	DDR data signal 40	I/O	
	AC27	PAD_MEM_DATA[41]	DDR data signal 41	I/O	
	AC28	PAD_MEM_DATA[42]	DDR data signal 42	I/O	
	AC25	PAD_MEM_DATA[43]	DDR data signal 43	I/O	
	AB25	PAD_MEM_DATA[44]	DDR data signal 44	I/O	
	AA26	PAD_MEM_DATA[45]	DDR data signal 45	I/O	
	AA27	PAD_MEM_DATA[46]	DDR data signal 46	I/O	
	AA28	PAD_MEM_DATA[47]	DDR data signal 47	I/O	
	AE29	PAD_MEM_DATA[48]	DDR data signal 48	I/O	
	AD29	PAD_MEM_DATA[49]	DDR data signal 49	I/O	
	C30	PAD_MEM_DATA[5]	DDR data signal 5	I/O	
	AD30	PAD_MEM_DATA[50]	DDR data signal 50	I/O	
	AE30	PAD_MEM_DATA[51]	DDR data signal 51	I/O	
	AA29	PAD_MEM_DATA[52]	DDR data signal 52	I/O	
	AA30	PAD_MEM_DATA[53]	DDR data signal 53	I/O	
	Y30	PAD_MEM_DATA[54]	DDR data signal 54	I/O	
	W30	PAD_MEM_DATA[55]	DDR data signal 55	I/O	
	AH27	PAD_MEM_DATA[56]	DDR data signal 56	I/O	
	AG28	PAD_MEM_DATA[57]	DDR data signal 57	I/O	
	AG27	PAD_MEM_DATA[58]	DDR data signal 58	I/O	
	AH28	PAD_MEM_DATA[59]	DDR data signal 59	I/O	
	F30	PAD_MEM_DATA[6]	DDR data signal 6	I/O	
	AE28	PAD_MEM_DATA[60]	DDR data signal 60	I/O	
	AD26	PAD_MEM_DATA[61]	DDR data signal 61	I/O	
	AD25	PAD_MEM_DATA[62]	DDR data signal 62	I/O	
	AD27	PAD_MEM_DATA[63]	DDR data signal 63	I/O	
	AK29	PAD_MEM_DATA[64]	DDR data signal 64	I/O	
	AJ27	PAD_MEM_DATA[65]	DDR data signal 65	I/O	
	AK27	PAD_MEM_DATA[66]	DDR data signal 66	I/O	
	AK28	PAD_MEM_DATA[67]	DDR data signal 67	I/O	

	AH30	PAD_MEM_DATA[68]	DDR data signal 68	I/O	
	AG29	PAD_MEM_DATA[69]	DDR data signal 69	I/O	
	E30	PAD_MEM_DATA[7]	DDR data signal 7	I/O	
	AG30	PAD_MEM_DATA[70]	DDR data signal 70	I/O	
	AF30	PAD_MEM_DATA[71]	DDR data signal 71	I/O	
	G25	PAD_MEM_DATA[8]	DDR data signal 8	I/O	
	F26	PAD_MEM_DATA[9]	DDR data signal 9	I/O	
	B29	PAD_MEM_DQS_N[0]	DDR data strobe signal 0N	I/O	
	F28	PAD_MEM_DQS_N[1]	DDR data strobe signal 1N	I/O	
	J27	PAD_MEM_DQS_N[2]	DDR data strobe signal 2N	I/O	
	H30	PAD_MEM_DQS_N[3]	DDR data strobe signal 3N	I/O	
	R29	PAD_MEM_DQS_N[4]	DDR data strobe signal 4N	I/O	
	AB28	PAD_MEM_DQS_N[5]	DDR data strobe signal 5N	I/O	
	AB30	PAD_MEM_DQS_N[6]	DDR data strobe signal 6N	I/O	
	AF27	PAD_MEM_DQS_N[7]	DDR data strobe signal 7N	I/O	
	AJ29	PAD_MEM_DQS_N[8]	DDR data strobe signal 8N	I/O	
	B30	PAD_MEM_DQS_P[0]	DDR data strobe signal 0P	I/O	
	F27	PAD_MEM_DQS_P[1]	DDR data strobe signal 1P	I/O	
	J28	PAD_MEM_DQS_P[2]	DDR data strobe signal 2P	I/O	
	J30	PAD_MEM_DQS_P[3]	DDR data strobe signal 3P	I/O	
	R30	PAD_MEM_DQS_P[4]	DDR data strobe signal 4P	I/O	
	AB27	PAD_MEM_DQS_P[5]	DDR data strobe signal 5P	I/O	
	AB29	PAD_MEM_DQS_P[6]	DDR data strobe signal 6P	I/O	
	AF28	PAD_MEM_DQS_P[7]	DDR data strobe signal 7P	I/O	
	AJ30	PAD_MEM_DQS_P[8]	DDR data strobe signal 8P	I/O	
	D30	PAD_MEM_DM[0]	DDR input data mask signal 0	I/O	
	E28	PAD_MEM_DM[1]	DDR input data mask signal 1	I/O	
	J26	PAD_MEM_DM[2]	DDR input data mask signal 2	I/O	
	L30	PAD_MEM_DM[3]	DDR input data mask signal 3	I/O	
	T30	PAD_MEM_DM[4]	DDR input data mask signal 4	I/O	
	AB26	PAD_MEM_DM[5]	DDR input data mask signal 5	I/O	
	AC30	PAD_MEM_DM[6]	DDR input data mask signal 6	I/O	
	AE27	PAD_MEM_DM[7]	DDR input data mask signal 7	I/O	
	AH29	PAD_MEM_DM[8]	DDR input data mask signal 8	I/O	
	AA25	PAD_MEM_CAL			

	W27	PAD_MEM_ADDRESS[0]	DDR address signal 0	I/O	
	N26	PAD_MEM_ADDRESS[1]	DDR address signal 1	I/O	
	V26	PAD_MEM_ADDRESS[10]	DDR address signal 10	I/O	
	Y28	PAD_MEM_ADDRESS[11]	DDR address signal 11	I/O	
	R26	PAD_MEM_ADDRESS[12]	DDR address signal 12	I/O	
	M25	PAD_MEM_ADDRESS[13]	DDR address signal 13	I/O	
	V25	PAD_MEM_ADDRESS[14]	DDR address signal 14	I/O	
	P25	PAD_MEM_ADDRESS[15]	DDR address signal 15	I/O	
	M26	PAD_MEM_ADDRESS[16]	DDR address signal 16	I/O	
	W28	PAD_MEM_ADDRESS[2]	DDR address signal 2	I/O	
	N25	PAD_MEM_ADDRESS[3]	DDR address signal 3	I/O	
	W25	PAD_MEM_ADDRESS[4]	DDR address signal 4	I/O	
	M28	PAD_MEM_ADDRESS[5]	DDR address signal 5	I/O	
	Y25	PAD_MEM_ADDRESS[6]	DDR address signal 6	I/O	
	L28	PAD_MEM_ADDRESS[7]	DDR address signal 7	I/O	
	Y27	PAD_MEM_ADDRESS[8]	DDR address signal 8	I/O	
	M27	PAD_MEM_ADDRESS[9]	DDR address signal 9	I/O	
	U27	PAD_MEM_CLK_N[0]	DDR differential clock signal 0N	I/O	
	T27	PAD_MEM_CLK_N[1]	DDR differential clock signal 1N	I/O	
	R27	PAD_MEM_CLK_N[2]	DDR differential clock signal 2N	I/O	
	P27	PAD_MEM_CLK_N[3]	DDR differential clock signal 3N	I/O	
	U28	PAD_MEM_CLK_P[0]	DDR differential clock signal 0P	I/O	
	T28	PAD_MEM_CLK_P[1]	DDR differential clock signal 1P	I/O	
	R28	PAD_MEM_CLK_P[2]	DDR differential clock signal 2P	I/O	
	P28	PAD_MEM_CLK_P[3]	DDR differential clock signal 3P	I/O	
	T26	PAD_MEM_ODT	DDR On-Die Termination signal, active high	O	
	V28	PAD_MEM_WE_N	DDR Write Enable signal, active low	O	
	R25	PAD_MEM_CS_N	DDR Chip Select signal, active low	O	
	N27	PAD_MEM_CAS_N	DDR Column Address Strobe signal, active low	O	
	T25	PAD_MEM_RAS_N	DDR Column Address Strobe signal, active low	O	
	W26	PAD_MEM_BANK[0]	DDR Bank Address 0	O	
	N28	PAD_MEM_BANK[1]	DDR Bank Address 1	O	
	V27	PAD_MEM_BANK[2]	DDR Bank Address 2	O	

	U25	PAD_MEM_CKE	DDR Clock Enable, active high	O	
	L27	PAD_MEM_RST_N	DDR reset, active low		
	L25	PAD_MEM_RETEN_N			
ADC	E3	ADC_A0			
	E4	ADC_B0			
Tsensor	E2	TS_VCM			
EFUSE	K7	VQPS18_EFUSE			

Notes:

(1) Default functions of the multiplexed signals are marked with an asterisk *.

4.2.2. Power supply

Table 4-3 Power supplies

Ball Ref.	Ball allocation	Description
VDD08_CPU	P9, P11, R8, R10, T9, U8, U10, V9, V11, W8, W10, W12	0.8V CPU/CPU1 PLL/CPU2 PLL power supply
VDD08_SOC	H13, H15, H17, H23, J10, J12, J14, J16, J18, J20, J22, K9, K11, K19, K21, L10, L12, L20, M9, M11, N8, N12, R12, T13, T15, T17, U14, U16, U18, V13, V15, V17, V19, W14, W16, W18, W20, Y9, Y11, Y13, Y15, Y17, Y19, AA10, AA12, AA14, AA16, AA18, AA20, AB13, AB17, AB19	0.8V SOC/SOC PLL/AI810 PLL/VPU PLL/DISPLAY PLL/HISS PLL/MIPI PLL power supply
VDD08_AI810	K13, K15, K17, L14, L16, L18, M13, M15, M17, M19, N14, N16, N18, N20, P13, P15, P17, P19, R14, R16, R18, R20	0.8V AI810 power supply
PLL_AVDD_CPU	T12	1.8V CPU1/CPU2 PLL power supply
PLL_AVDD2_CPU1	T11	0.8V CPU1 PLL power supply
PLL_AVDD2_CPU2	U12	0.8V CPU2 PLL power supply
PLL_AVSS	H18, P10, T20, U11, U19, AC12	PLL ground
VDDIO_SOC	F4, F15, F17 G12, G14, G16, J4, M7, N6, P7, R6, U6, V7, W6	1.8V /3.3V SOC IO power supply
PLL_AVDD	H19, N10, R19, AC13	1.8V SOC PLL/AI810 PLL/VPU PLL/DISPLAY PLL/HISS PLL/MIPI PLL/AUD PLL power supply
PLL_AVDD2_SOC	N11	0.8V SOC PLL power supply
PLL_AVDD2_AI810	T18	0.8V AI810 PLL power supply
PLL_AVDD2_VPU	T19	0.8V VPU PLL power supply

PLL_AVDD2_DISPLAY	G18	0.8V DISPLAY PLL power supply
PLL_AVDD2_HSIO	AD12	0.8V HISS PLL power supply
PLL_AVDD2_TSEN	AD13	0.8V MIPI PLL power supply
PLL_AVDD2_AUD	N9	0.8V AUD PLL power supply
VDD08_DDR	L22, M21, N22, P21, R22, T21, U22, V21, W22, Y21, AA22, AB21, AB23	0.8V DDR/DDR PLL power supply
VDDIO_DDR	E26, G24, H26, J24, K23, L26, M23, P23, P26, R24, T23, U26, V23, Y23, Y26, AC24, AC26	1.2V/1.35V/1.5V DDR IO power supply
VSSIO_DDR	C28, E29, H24, H29, L23, L29, N23, P29, R23, T24, U23, U29, W23, Y29, AA23, AB24, AC29, AD24, AE26, AF29, AJ28	DDR IO ground
PAD_MEM_VREF[0]	K24	DDR reference voltage
PAD_MEM_VREF[1]	L24	DDR reference voltage
PAD_MEM_VREF[2]	M24	DDR reference voltage
PAD_MEM_VREF[3]	N24	DDR reference voltage
PAD_MEM_VREF[4]	P24	DDR reference voltage

PAD_MEM_VREF[5]	U24	DDR reference voltage
PAD_MEM_VREF[6]	V24	DDR reference voltage
PAD_MEM_VREF[7]	W24	DDR reference voltage
PAD_MEM_VREF[8]	Y24	DDR reference voltage
PAD_MEM_VREF[9]	AA24	DDR reference voltage
PLL_AVDD_DDR	U20	1.8V DDR PLL power supply
PLL_AVDD2_DDR	U21	0.8V DDR PLL power supply
AVDD08_PCIE	AB11	0.8V PCIE power supply
AVDD08_PCIE_TX0	AD8	0.8V PCIE VPTX0 power supply
AVDD08_PCIE_TX1	AD9	0.8V PCIE VPTX1 power supply
AVDD08_PCIE_TX2	AD10	0.8V PCIE VPTX2 power supply
AVDD08_PCIE_TX3	AD11	0.8V PCIE VPTX3 power supply
AVDD18_PCIE	AB10	1.8V PCIE IO power supply
PCIE_RESREF	AH5	PCIE reference voltage
AVDD08_SRIO	AA9	0.8V SRIO CM & SRIO power supply
AVDD08_SRIO_AVTT0	Y7	0.8V SRIO AVTT0 power supply
AVDD08_SRIO_AVTT1	AA7	0.8V SRIO AVTT1 power supply
AVDD08_SRIO_AVTT2	AB7	0.8V SRIO AVTT2 power supply
AVDD08_SRIO_AVTT3	AC7	0.8V SRIO AVTT3 power supply
AVDD18_SRIO	AB9	1.8V SRIO CM power supply
SRIO_RESREF	AA3	RapidIO reference voltage
VDD08_LVDS	H21	0.8V LVDS power supply
AVDD18_LVDS	G20	1.8V LVDS power supply
AVDD25_LVDS	G22	2.5V LVDS power supply
AVSS_LVDS	A16, A27, B16, B27, C16, C17, C18, C19, C20, C21, C23, C24, C25, C26, C27	LVDS C/IO ground
VDD08_MIPI	AB15, AC14	0.8V MIPI power supply
AVDD18_MIPI	AD14, AD15	1.8V MIPI IO power supply
AVSS_MIPI	AH10, AH11, AH12, AH13, AJ8, AK14	MIPI ground
AVDD18_USB0	H11	1.8V USB0 power supply
AVDD18_USB1	H9	1.8V USB1 power supply
AVDD33_USB0	G10	3.3V USB0 power supply
AVDD33_USB1	G8	3.3V USB0 power supply
VDD08_CMLK	AC17, AC19, AC20, AC22	0.8V camera link power supply
AVDD18_CMLK_BASE	AD18	1.8V camera link BASE power supply
AVDD25_CMLK_BASE	AD19	2.5V camera link BASE power supply
AVDD18_CMLK_MEDI	AD21	1.8V camera link MEDI power supply
AVDD25_CMLK_MEDI	AD22	2.5V camera link MEDI power supply
AVDD18_CMLK_FULL	AE23	1.8V camera link FULL power supply
AVDD25_CMLK_FULL	AE24	2.5V camera link FULL power supply
AVDD18_CMLK_TX	AE16	1.8V camera link TX power supply
AVDD25_CMLK_TX	AD16	2.5V camera link TX power supply
AVDD18_CMLK_BUF_BASE	AD17	1.8V camera link VCCBUF BASE power supply
AVDD18_CMLK_BUF_MEDI	AD20	1.8V camera link VCCBUF MEDI power supply
AVDD18_CMLK_BUF_F	AD23	1.8V camera link VCCBUF FULL

ULL		power supply
AVSS_CMLK	AE14, AE17, AE18, AE19, AE20, AE21, AE22, AE25, AF20, AF26, AG20, AG26, AH14, AH15, AH16, AH17, AH18, AH19, AH20, AH21, AH22, AH23, AH24, AH25, AH26, AJ14, AJ20, AJ26, AK20, AK26	Camera link BASE/MEDI/FULL/TX ground
VDD08_RTC	J8	0.8V RTC power supply
AVDDH33	H7	3.3V RTC power supply
AVDD18	L8	1.8V PVTSENSOR/ADC/POR power supply
ADC_VREFH	D3	ADC reference voltage high
ADC_VREFL	D4	ADC reference voltage low
VDDIO18_OSC	T7	1.8V OSC power supply
VDD33_SDIO	F9	3.3V SDIO power supply
VDDIO_NF	F11	3.3V/1.8V NF IO power supply
VDDIO_PERI	F13	3.3V/1.8V PERI IO power supply
VQPS18_EFUSE	K7	1.8V EFUSE power supply
VSS	B9, B12, B15, E21, E25 F3, G13, G15, G17, G19, G21, G23, H12, H14, H16, H20, H22, J3, J9, J13, J15, J17, J19, J21, J23, K8, K10, K12, K14, K16, K18, K20, K22, L9, L11, L13, L15, L17, L19, L21, M8, M10, M12, M14, M16, M18, M20, M22, N1, N2, N7, N13, N15, N17, N19, N21, P3, P8, P12, P14, P16, P18, P20, P22, R3, R7, R9, R11, R13, R15, R17, R21 T3, T8, T10, T14, T16, T22, U3, U7, U9, U13, U15, U17, V1, V2, V8, V10, V12, V14, V16, V18, V20, V22 W3, W7, W9, W11, W13, W15, W17, W19, W21, Y3, Y8, Y10, Y12, Y14, Y16, Y18, Y20, Y22, AA8, AA11, AA13, AA15, AA17, AA19, AA21, AB3, AB8, AB12, AB14, AB16, AB18, AB20, AB22, AC3, AC8, AC9, AC10, AC11, AC15, AC16, AC18, AC21, AC23, AD1, AD2, AD5, AD7 AE3, AF3, AF7, AF10,	Ground

	AG3, AH3, AH4, AH6, AH7, AJ1, AJ2, AK2, AK8	
AVSS	B3, B5, E5, G7, G9, G11, H8, H10 J7, L7	Ground

Note:

For reference value of related power supply voltage range, please refer to chapter 5 for details

5. OPERATING CONDITIONS AND ELECTRICAL CHARACTERISTICS

5.1. PVT sensor

5.1.1. Maximum ratings

Table 5-1 PVT sensor maximum ratings

Parameter description	Symbol	Min.	Typ.	Max.	Unit
AVDD/DVDD18 supply voltage		1.62	1.8	1.98	V
DVDD supply voltage		0.72	0.8	0.88	V
Sensor temperature range		-40	25	125	℃
Operating current (F CLK =100KHz)	I_{OP}		250		uA
Power shutdown current	I_{PD}		2.5		uA
Data conversion time (F CLK =100KHz)	T_{CONV}		350		ms
Clock output frequency	F_{CLK}	10	100	200	uA

5.1.2. Temperature sensor characteristics

Table 5-2 PVT sensor temperature sensor characteristics

Parameter description	Symbol	Min.	Typ.	Max.	Unit
Temperature measurement range	T_{RNG}	-40		125	℃
Resolution	T_{RSLT}		0.1		℃/LSB
Measurement error	T_{INACC}		±5		℃

5.1.3. Voltage sensor characteristics

Table 5-3 PVT sensor voltage sensor characteristics

Parameter description	Symbol	Min.	Typ.	Max.	Unit
Voltage measurement range	V_{RNG}	0.7		1.0	V
Resolution	V_{RSLT}		0.5		mV/LSB
Measurement error	V_{INACC}		±40		mV

5.2. SAR ADC

5.2.1. Electrical characteristics

Table 5-4 electrical characteristics

Parameter description		Min.	Typ.	Max.	Unit
Resolution			12		bit
Junction temperature (operating)		-40		125	℃
Voltage supply					
AVDD18 Voltage supply		1.62	1.8	1.98	V
DVDD08 Voltage supply		0.72	0.8	0.88	V
Operating current @1Msps			100		uA
Stand-by current			10		uA
Current consumption in power-off mode			1		uA
Analog inputs					
Sampling input capacitance (Cs)			3		pF
Sampling input resistance (Rs)	SEL_SPEED=0	2250	3000	4000	Ω
	SEL_SPEED=1	420	600	800	Ω
VREFH			1.8	AVDD	V
VREFL		0		0.1	V
Input range (single-ended mode)		VREFH - VREFL			V
Input range (differential mode)		2*(VREFH - VREFL)			Vpp
Performance					
DNL			±1.5		LSB
INL			±3		LSB
SNR @Fin=20KHz 1MSPS			62		dB
THD @Fin=20KHz 1MSPS			-62		dB
Offset error before calibration			+/- 25		LSB
Offset error after calibration			+/-5		LSB
Timing characteristics					
Input clock frequency (Fclk)			16	80	MHz
Clock duty cycle		45	50	55	%
Conversion cycle (tc))			16		CLK
Sampling rate (Fs	SEL_SPEED=0			1	MSPS
	SEL_SPEED=1			5	MSPS

SOC input time (tSOC)		6		ns
SOC setting time before the rising edge of CLK (tsocst)		0.1	1	ns
SOC holding time after the rising edge of CLK (Tsochld)		1	2	ns
Delay time from rising edge of CLK to EOC		3	4.5	ns
Delay time from rising edge of CLK to falling edge of EOC (teocf)		3	4.5	ns
EOC width (teocw)	1			CLK
Valid data output delay after the rising edge of EOC (tdata)		4	6	ns
Power-off mode start time		5		μs

5.3. RTC Real Time Clock

5.3.1. Maximum ratings

Table 5-5 Maximum ratings

Parameter description	Symbol	Min.	Typ.	Max.	Unit	Notes
Power supply - Analog	AVDDH	1.8	3.3	3.63	V	
Power supply - Digital	DVDD	0.72	0.8	0.88	V	Crystal specified range
Ambient temperature	TA	-40	25	85	°C	
Junction temperature	TJ	-40	25	125	°C	
CLK_OSCL output clock voltage	VOL		0		V	
	VOH		DVDD		V	
CLK_OSC output clock voltage	VOL		0		V	VCC_XO=1.2V~2 V VCC_XO no supply current capability
	VOH		VCC_XO		V	
CLK_OSCL output frequency	fOSC	-20ppm	F0	+20ppm	Hz	T_A=25°CVDDH=3.3V F0:32768HZ
Frequency stability of CLK_OSCL and AVDDH	Δf1/fOSC/ΔV	-3		+3	ppm/V	T_A=25°C
Frequency stability rate	Δf1/fOSC	-100			ppm	-20/+70°C
		-200				-40/+85°C
Output duty cycle	D	40	50	60	%	Dynamic mode
		D_O-5	D_O	D_{O+5}	%	Bypass mode. The duty cycle of the clock input is DO%
RTC start time	T_{ON1}		300	1000	ms	Depends on AVDDH level, power-on speed, oscillator type and temperature
RTC time deviation per day	T_{DEN}	1			s	At 25°C
Operating current	I_{VCC33}		1.5	10	uA	Average current
Bypass mode frequency	f_{bypass}	20k	32768	100k	Hz	XIN32K is directly connected to an external clock (square or sine waveforms)
Bypass mode swing	Vpp_{bypass}	0.3	1	1.2	V	

Bypass mode current	I_{bypass}		1.5	10	uA	Input 20KHz~100KHz waveform with Vpp=1V
Bypass mode start time	T_{ON2}		2		ms	Input 20KHz~100KHz waveform with Vpp=1V

6. SYSTEM OPERATION

6.1. Reset

SoC reset operation diagram

Table 6-1 SoC reset command

Symbol	Description
POR	Chip internal Power-On-Reset
RESETN	Off-chip reset
HW_RSTN	Hardware reset
WDT_SW_RSTN	Software watchdog reset
WDT_RSTN	Watchdog reset output
SYS_RSTN	System reset
BLK_SW_RSTN	Software control sub-module reset

Table 6-2 SoC reset operation commands

Reset type	Operation	Description
Global hard reset	External reset and internal power-on reset POR module	Global reset SOC
Chip watchdog reset	Chip watchdog module	Perform a global reset on the SOC except the watchdog itself
Software control sub-module reset	Software configuration sub-module reset control bit	Individual reset of each sub-module of the SOC.

6.2. Clock

6.2.1. Clock input sources

Yulong810A has five types system clock input sources:

1) One 24MHz oscillator, used as primary clock source for the PLLs, to generate the clock for CPU, AI810, VPU, DDR, BUS, high-speed interfaces, etc. For all PLLs, the 24MHz clock from the oscillator can be used as the PLL reference clock directly;
2) One 32KHz oscillator, used as the clock source for RTC;
3) One 62.5MHz for Rapid IO reference clock;
4) One 100MHz for PCIe reference clock.

6.2.2. PLL Distribution

In order to meet the clock requirement for each IP blocks, Yulong810A provides following PLLs:

- PLL_CPU0, used to generate the clock for ARM Cortex-A9 platform;
- PLL_CPU1, used to generate the clock for SPARC LEON4 platform;
- PLL_AI810, used to generate the clock for GPU;
- PLL_VPU, used to generate the clock for VPU;
- PLL_SOC: used to generate the clock for SOC, including BUS, HSIO, peripherals, etc;
- PLL_DDR: used to generate the clock for DRAM PHY and controller;
- PLL_DISP: used to generate the clock for video output display interface;
- PLL_SENS: used to generate the clock for video input sensor interface;
- PLL_HSIO: used to generate the clock for high speed interface;
- PLL_AUD, used to generate the clock for audio interfaces.

Three PLLs are included in sub-block to reduce jitter on the clock path:

- PLL_CPU0 is put close to the Quad CA9 platform hard block to minimize the jitter;
- PLL_CPU1 is put close to the Quad SPARC platform hard block to minimize the jitter;
- PLL_DDR is put close to the DDR PHY to minimize the clock jitter. To make it easier for the interface to meet the jitter requirement in JEDEC standard.

Two types of PLLs are used:

- Integer PLLs : PLL_CPU0, PLL_CPU1, PLL_AI810, PLL_VPU, PLL_SOC, PLL_SENS and PLL_HSIO are integer PLLs; frequency configurable;
- Fractional PLLs: PLL_DDR, PLL_DISP, PLL_AUD; can be configured to very accurate frequency required by audio and video interfaces.

Each PLL has its dedicated configuration register, which can be accessed through the APB bus. The software can enable/disable the phase-locked loop or change its clock frequency.

All the fractional PLL can support on-the-fly frequency adjustment in small steps without glitch on its clock output. In addition to the register interface, each PLL also has a dedicated pll_enable input and pll_lock output to support PLL disable/enable control from CCM.

6.2.3. Clock structure block diagram

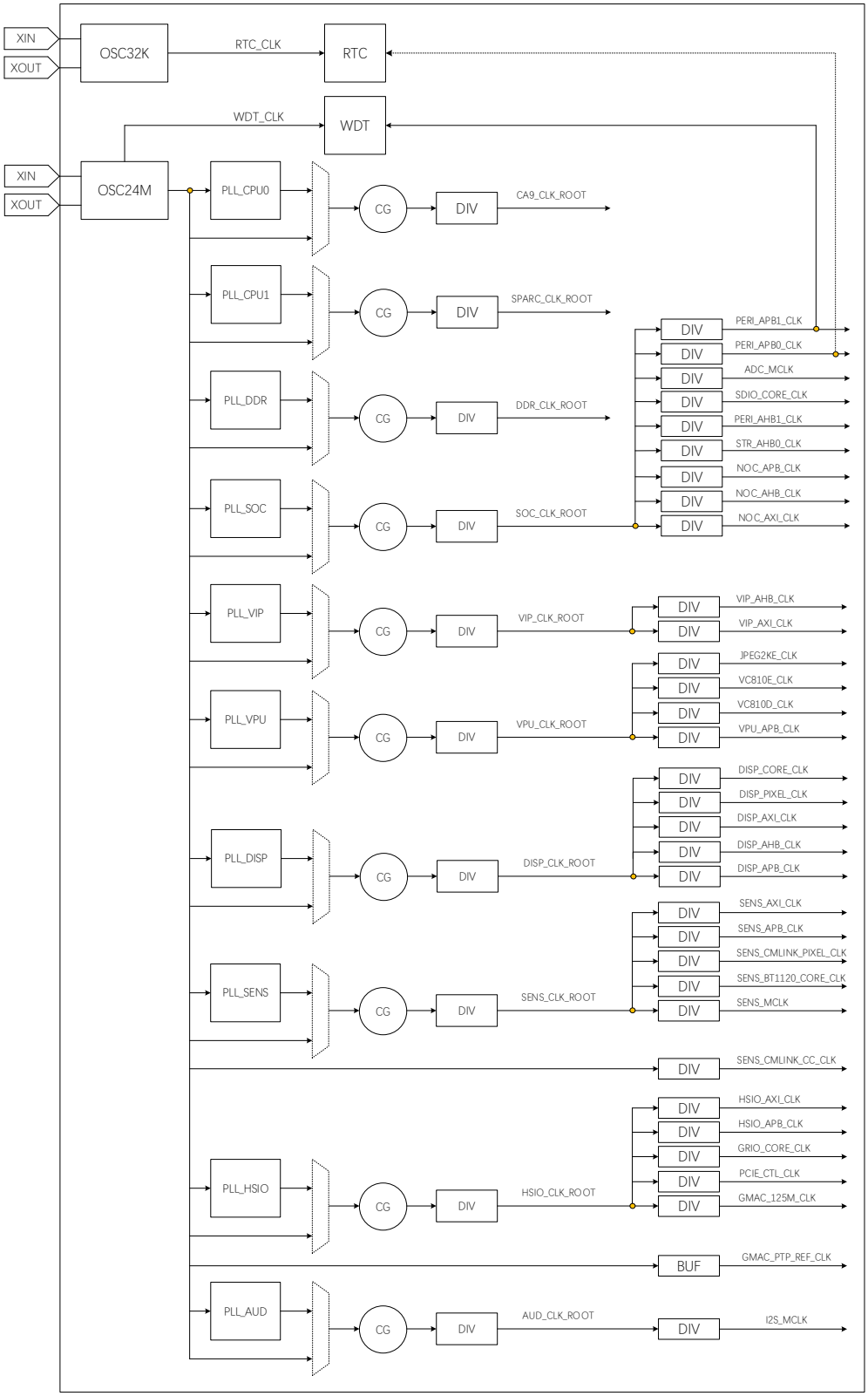

Figure 6-1 SoC clock structure block diagram

6.2.4. PLL Configuration Program Flow

PLL Max Frequency (output frequency supported by each PLL):

Table 6-3 PLL Max Frequency

PLL	Type	VCO Freq (MHz)	Pre-Divider	Post-Divider	PLL Freq (MHz)	Description
PLL_CPU0	Integer	800~3200	1~7	1~8	1000	CA9 CPU platform
PLL_CPU1	Integer	800~3200	1~7	1~8	800	SPARC CPU platform
PLL_AI810	Integer	800~3200	1~7	1~8	800	AI810 Subsystem
PLL_VPU	Integer	800~3200	1~7	1~8	750	VPU Subsystem
PLL_SENS	Integer	800~3200	1~7	1~8	700	Sensor Subsystem
PLL_HSIO	Integer	800~3200	1~7	1~8	750	HSIO Subsystem
PLL_SOC	Integer	800~3200	1~7	1~8	800	SoC Top
PLL_DDR	Fractional	800~3200	1~7	1~8	2667	DDR Subsystem
PLL_DISP	Fractional	800~3200	1~7	1~8	900	Display Subsystem
PLL_AUD	Fractional	800~3200	1~7	1~8	300	Audio I2S I/F

6.2.5. Subsystem maximum frequency

Maximum frequency supported for each subsystem clock.

Table 6-4 Subsystem max frequency

PLL	Block	Target Clock (MHz)		Divider	Source Clock (MHz)	
		Name	Fmax		Name	Fmax
XTAL_24M		xtal_clk24m	24	na	na	na
XTAL_32K		xtal_clk32k	0.032	na	na	na
PLL_CPU0	ca9mp_cpu	ca9mp_clk	1000	1~8	ca9mp_pll_clk	1000
		ca9mp_periphclk	1000	1~8	ca9mp_clk	1000
		ca9l2_clk	450	1~8	ca9mp_clk	1000
		cssys_traceclk	150	1~8	ca9mp_pll_clk	1000
PLL_CPU1	sparc_cpu	Sparc_clk	800	1~8	Sparc_pll_clk	800
PLL_AI810	AI810	AI810core_clk	800	1~8	pll_AI810_clk	800
		AI810axi_clk	800	1~8	pll_AI810_clk	800
		AI810ahb_clk	200	1~8	pll_AI810_clk	800
PLL_VPU	vc810d	vc810d_aclk	375	1~8	pll_vpu_clk	750

		vc810d_pclk	125	1~8	pll_vpu_clk	750
	vc810e	vc810e_aclk	375	1~8	pll_vpu_clk	750
		vc810e_pclk	125	1~8	pll_vpu_clk	750
	jpeg2000e	jpeg2000e_aclk	750	1~8	pll_vpu_clk	750
		jpeg2000e_pclk	125	1~8	pll_vpu_clk	750
PLL_SENS	cameralink	cmlk_aclk	350	1~8	pll_sens_clk	700
		cmlk_pclk	140	1~8	pll_sens_clk	700
		cmlk_pixclk	350	1~8	pll_sens_clk	700
		cmlk_ccclk	2	1~128	xtal_clk24m	24
	mipi csi-2	mipi_aclk	350	1~8	pll_sens_clk	700
		mipi_pclk	140	1~8	pll_sens_clk	700
		mipi_cfgclk	27	1~64	pll_sens_clk	700
	bt1120	bt1120_aclk	350	1~8	pll_sens_clk	700
		bt1120_pclk	140	1~8	pll_sens_clk	700
	sensor	sens_mclk	27	1~64	pll_sens_clk	700
PLL_HSIO	pcie	pcie_aclk	375	1~8	pll_hsio_clk	750
		pcie_aux_clk	24	na	xtal_clk24m	24
	grio	grio_core_clk	375	1~8	pll_hsio_clk	750
		grio_ctl_clk	750/8	1~32	pll_hsio_clk	750
	gmac	gmac_aclk	375	1~8	pll_hsio_clk	750
		gmac_clk125m	125	1~8	pll_hsio_clk	750
		gmac_pclk	125	1~8	pll_hsio_clk	750
		gmac_ptp_ref_clk	24	na	xtal_clk24m	24
	hsio	hsio_pclk	125	1~8	pll_hsio_clk	750
PLL_SOC	noc	noc_aclk	400	1~8	pll_soc_clk	800
		noc_hclk	200	1~8	pll_soc_clk	800
		noc_pclk	100	1~8	pll_soc_clk	800
	storage	ahb0_hclk	200	1~8	pll_soc_clk	800
	Peripheral	ahb1_hclk	200	1~8	pll_soc_clk	800
		apb0_pclk	100	1~8	ahb1_hclk	200
		apb1_pclk	100	1~8	ahb1_hclk	200
	sdio	sdio_cclk_in	200	1~8	pll_soc_clk	800
		sdio_tmclk	24	na	xtal_clk24m	24
	usb	usb_internalclk	24	na	xtal_clk24m	24
		usb_adp_clk	0.032	na	rtc_clk32k	0.032

	wdt	wdt_clk	24	na	xtal_clk24m	24
	adc	adc_mclk	80	1~32	pll_soc_clk	800
	pvt_sensor	pvt_clk_in	0.032	na	rtc_clk32k	0.032
PLL_DDR	ddr	ddr_phy_ddr_clk	1333	2	pll_out_ddr_clk	2667
		drc_core_clk	667	2	ddr_phy_clk	1333
PLL_DISP	dc8000	dc8000_aclk	450	1~8	pll_disp_clk	900
		dc8000_hclk	225	1~8	pll_disp_clk	900
		dc8000_core_clk	450	1~8	pll_disp_clk	900
		dc8000_pixel_clk	150	1~64	pll_disp_clk	900
	display	disp_pclk	150	1~8	pll_disp_clk	900
PLL_AUD	i2s	i2s_mclk	100	1~256	pll_aud_clk	300

6.3. Power Management and Low Power Mode

6.3.1. Power supply architecture

The power architecture of the chip is defined based on the assumption that external PMIC is always used to supply all the power rails to the processor.

The digital logic inside chip will be supplied with 5 supplies. All of the VDD supplies are at nominal voltage, except for VDD_AI810 with OD voltage.

- VDD_CPU is for the Cortex-A9 platform and SPARC LEON platform.
- VDD_AI810 is for the AI810 only.
- VDD_DDR is for the DDR controller & PHY.
- VDD_RTC is for the RTC always-on part.
- VDD_SOC is for rest of the modules in SoC.

1. The GPIO pads will have external power supply for 3.3V and 1.8V IO voltage. The IO pad core voltage will be supplied directly by VDD_SOC (except for RTC IO).
2. The DDR controller & PHY have two external power supplies, VDD_DDR for controller & PHY, and VDDIO_DDR for IO.
3. For all the integrated analog modules, their 1.8V analog power and 0.8V digital power will be supplied externally through power pads. These supplies are separated with other power pads on the package to keep them clean, but they can be shared with other power rails on the board to reduce the number of power supplies from the PMIC.
4. For all the integrated PCIe PHY, MIPI PHY, Camera Link PHY, Rapid IO PHY, LVDS TX PHY, SDEMMC PHY and USB20 PHY, their 3.3V, 2.5V, 1.8V and 0.8V power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be shared with other power rails on the board to reduce the number of power supplies from the PMIC.
5. For RTC, the 0.8V core logic supply and 3.3V analog/IO supply will be supplied externally.
6. There are no integrated LDOs inside the chip (except for Analog PHY internal LDO).

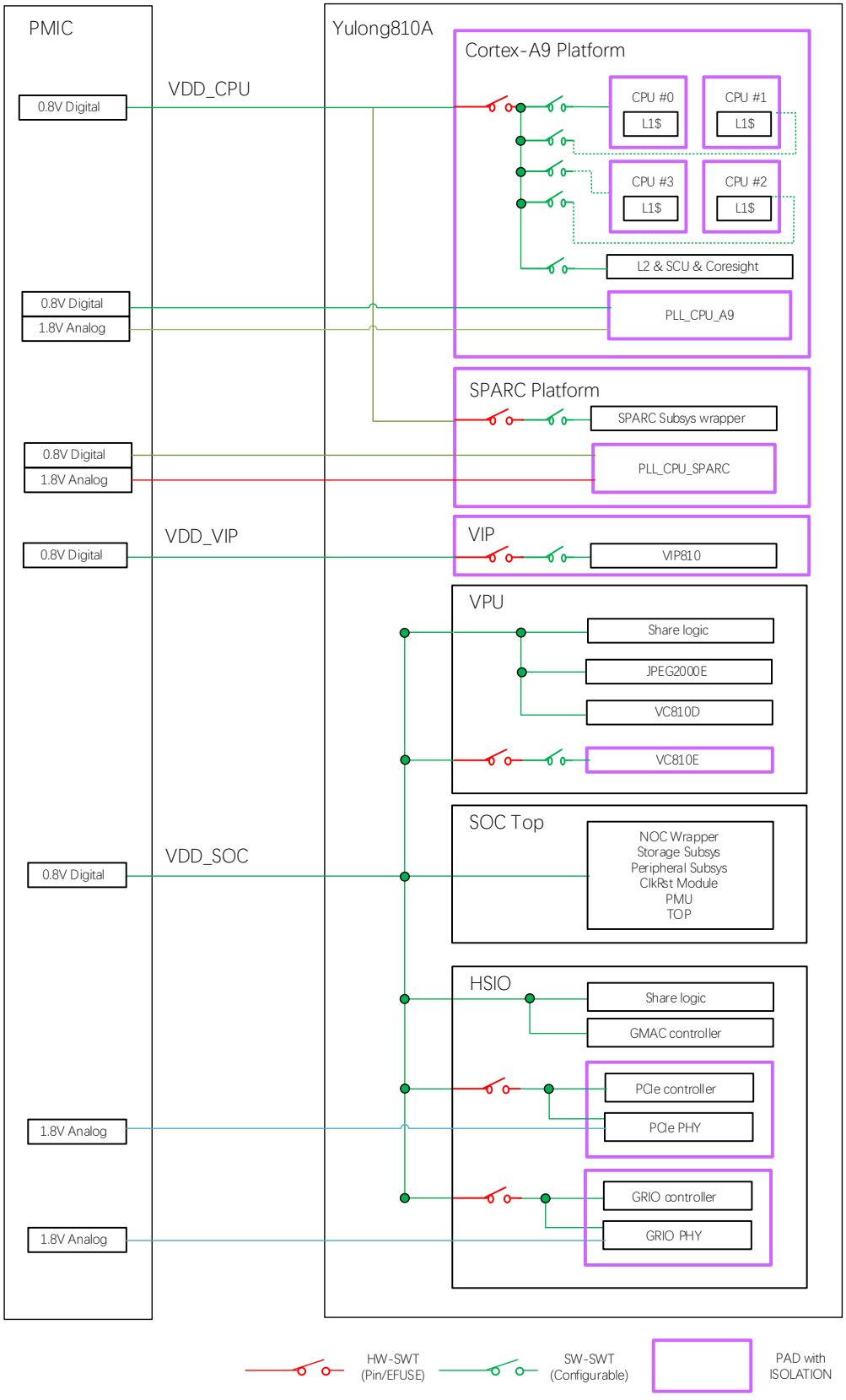

Figure 6-2 SoC Power supply block diagram (a)

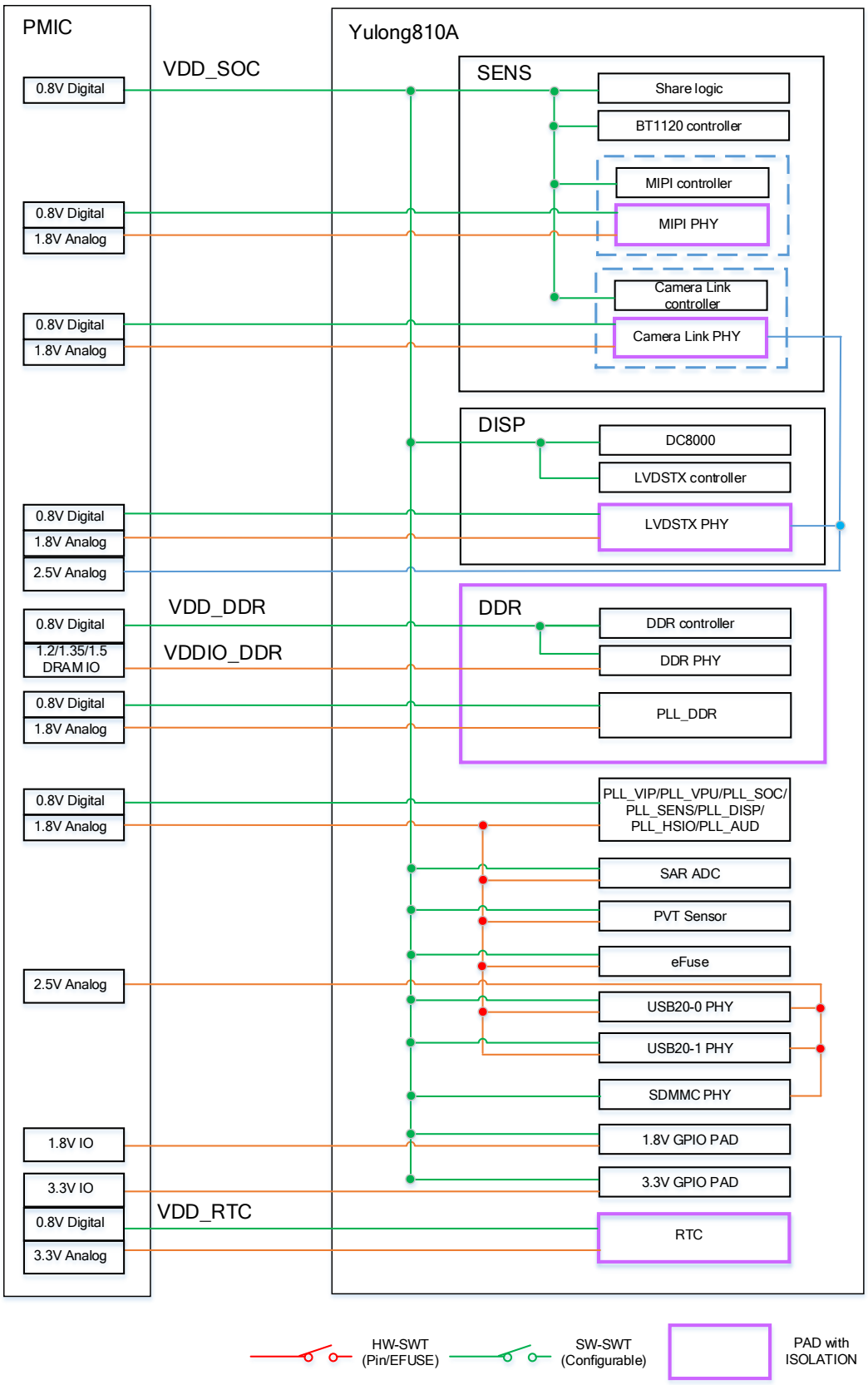

Figure 6-3 SoC Power supply block diagram (b)

6.3.2. Power supply characteristics

Yulong810A needs external PMIC to provide power supply as follows.

- 1.8V power supply for Analog Macro and IO.
- 3.3V power supply for USB2.0 PHY, SDEMC PHY and IO.
- 0.8Vpower supply for the core logic.

Table 6-5 Power supply characteristics

Power supply	Vmin (V)	Vtyp (V)	Vmax (V)	Description
VDD_CPU	0.72	0.80	0.88	CPU power supply
VDD_AI810	0.72	0.80	0.88	AI810-OI power supply
VDD_SOC	0.72	0.80	0.88	SoC logic power supply
VDD_DDR	0.72	0.80	0.88	DDRC power supply
VDD_RTC	0.72	0.80	0.88	RTC power supply
VDDA_1P8_CA9	1.62	1.80	1.98	CA9 PLL 1.8V power supply
VDDA_1P8_SPARC	1.62	1.80	1.98	SPARC PLL 1.8V power supply
VDDA_1P8_DDR	1.62	1.80	1.98	DDR PLL 1.8V power supply
VDDA_1P8_PCIE_PHY	1.62	1.80	1.98	PCIE PHY 1.8V power supply
VDDA_1P8_GRIO_PHY	1.62	1.80	1.98	GRIO PHY 1.8V power supply
VDDA_0P8_DPHY	0.72	0.80	0.88	MIPI DPHY 0.8V power supply
VDDA_1P8_DPHY	1.62	1.80	1.98	MIPI DPHY 1.8V power supply
VDDA_0P8_CMLK_PHY	0.72	0.80	0.88	Camera Link PHY 0.8V power supply
VDDA_1P8_CMLK_PHY	1.62	1.80	1.98	Camera Link PHY 1.8V power supply
VDDA_2P5_CMLK_PHY	2.25	2.50	2.75	Camera Link PHY 2.5V power supply
VDDA_0P8_LVDS_PHY	0.72	0.80	0.88	LVDS PHY 0.8V power supply
VDDA_1P8_LVDS_PHY	1.62	1.80	1.98	LVDS PHY 1.8V power supply
VDDA_2P5_LVDS_PHY	2.25	2.50	2.75	LVDS PHY 2.5V power supply
VDDA_1P8_SOC	1.62	1.80	1.98	SOC Analog Macro 1.8V power supply
VDDA_3P3_SOC	2.97	3.30	3.63	USB SDEV PHY.3V power supply
VDDA_3P3_RTC	1.80	3.30	3.63	RTC Analog Macro 3.3V power supply
VDDIO_1P8	1.62	1.80	1.98	1.8V GPIO PAD 1.8V power supply
VDDIO_3P3	2.97	3.30	3.63	3.3V GPIO PAD 3.3V power supply
VDDIO_3P3_RTC	2.97	3.30	3.63	3.3V RTC PAD 3.3V power supply
VDDIO_DRAM	1.14	1.20	1.26	DDR4 power supply
	1.14	1.20	1.30	LPDDR3 power supply
	1.425	1.50	1.575	DDR3 power supply
	1.283	1.35	1.45	DDR3L power supply

6.3.3. Maximum power

The maximum power target for each power supply is defined in Table 6-6 Maximum power

Table 6-6 Maximum power consumption

Power supply	Max. current consumption	Note
VDD_CPU	3000mA	Maximum power target
VDD_AI810	12000mA	Maximum power target
VDD_SOC	10000mA	Maximum power target
VDD_DDR	3000mA	Maximum power target
VDD_RTC	100uA	Maximum power target
VDDA_1P8_CA9	10mA	Maximum power target
VDDA_1P8_SPARC	10mA	Maximum power target
VDDA_1P8_DDR	10mA	Maximum power target
VDDA_0P8_PCIE_PHY	155mA	Maximum power target
VDDA_1P8_PCIE_PHY	65mA	Maximum power target
VDDA_0P8_GRIO_PHY	400mA	Maximum power target
VDDA_1P8_GRIO_PHY	140mA	Maximum power target
VDDA_0P8_DPHY	25mA	Maximum power target
VDDA_1P8_DPHY	15mA	Maximum power target
VDDA_0P8_CMLK_PHY	15mA	Maximum power target
VDDA_1P8_CMLK_PHY	135mA	Maximum power target
VDDA_2P5_CMLK_PHY	130mA	Maximum power target
VDDA_0P8_LVDS_PHY	15mA	Maximum power target
VDDA_1P8_LVDS_PHY	85mA	Maximum power target
VDDA_2P5_LVDS_PHY	90mA	Maximum power target
VDDA_1P8_SOC	100mA	Maximum power target
VDDA_3P3_SOC	150mA	Maximum power target
VDDA_3P3_RTC	100uA	Maximum power target
VDDIO_3P3_RTC	100uA	Maximum power target
VDDIO_1P8	TBD	Target to be determined by : Imax = N x C x V x (0.5 x F) with N: Number of IO pins powered by the power rail C: Equivalent external capacitive load. V: IO voltage. (0.5 xF): Data change rate, up to 0.5 clock.
VDDIO_3P3	TBD	
VDDIO_DRAM	TBD	
	TBD	
	TBD	
	TBD	

6.3.4. Power modes

SoC supports the following power modes:

- RUN Mode: In this mode, the Quad-Cortex A9 CPU core and Quad-Cortex A9 CPU core are active and running, some portion can be shut off for power saving.
- IDLE Mode: This mode is defined as a mode which CPU can automatically enter when there is no thread running. All high-speed devices are not active, DRAM & bus clock are reduced, most of the internal logic is clock gated but still remain powered. Compared to operating mode, all the external power supplies from PMIC remain unchanged, and most of the IP modules maintain same state, so the interrupt response latency in this mode is very short.
- SUSPEND Mode: This mode is defined as the most power saving mode where all the clocks are off and all the unnecessary power supplies are off. Cortex A9 CPU platform and SPARC V8 platform are fully power gated, all internal digital logic & analog circuit that can be power down will be off, all PHYs are power gated (Note: Analog and PHY need external power gating). The exit time from this mode will be much longer than IDLE mode but the power consumption will also be much lower.
- RTC Mode: In this mode, only the power for the RTC domain remain on to keep RTC logic alive.
- OFF Mode: This mode has all power rails OFF.

Low power mode:

The IDLE, SUSPEND, RTC mode are referred as low power mode for the chip. IDLE and SUSPEND are the two typical low power mode based on the use case of Linux kernel. The following table summarizes the external power supply state in all power mode.

Table 6-7 Low power modes

Power supply	OFF	RTC	SUSPEND	IDLE	RUN
VDD_CPU	OFF	OFF	OFF	ON	ON
VDD_AI810	OFF	OFF	OFF	ON	ON
VDD_DDR	OFF	OFF	OFF	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDD_RTC	OFF	ON	ON	ON	ON
VDDA_1P8_CA9	OFF	OFF	OFF	ON	ON
VDDA_1P8_SPARC	OFF	OFF	OFF	ON	ON
VDDA_1P8_DDR	OFF	OFF	OFF	ON	ON
VDDA_1P8_PCIE_PHY	OFF	OFF	OFF	ON	ON
VDDA_1P8_GRIO_PHY	OFF	OFF	OFF	ON	ON
VDDA_0P8_DPHY	OFF	OFF	OFF	ON	ON
VDDA_1P8_DPHY	OFF	OFF	OFF	ON	ON
VDDA_0P8_CMLK_PHY	OFF	OFF	OFF	ON	ON
VDDA_1P8_CMLK_PHY	OFF	OFF	OFF	ON	ON
VDDA_2P5_CMLK_PHY	OFF	OFF	OFF	ON	ON
VDDA_0P8_LVDS_PHY	OFF	OFF	OFF	ON	ON

VDDA_1P8_LVDS_PHY	OFF	OFF	OFF	ON	ON
VDDA_2P5_LVDS_PHY	OFF	OFF	OFF	ON	ON
VDDA_1P8_SOC	OFF	OFF	ON	ON	ON
VDDA_3P3_SOC	OFF	OFF	ON	ON	ON
VDDA_3P3_RTC	OFF	ON	ON	ON	ON
VDDIO_1P8	OFF	OFF	ON	ON	ON
VDDIO_3P3	OFF	OFF	ON	ON	ON
VDDIO_3P3_RTC	OFF	ON	ON	ON	ON
VDDIO_DRAM	OFF	OFF	ON	ON	ON

6.3.5. Power domain

In order to optimize the power consumption in low power modes, Yulong810A has multiple power domains. This allows most of SOC digital and analog logics to be power gated with internal power switch or external supply from PMIC in low power mode.

Table 6-8 Power domain

Power domain	Supplied by	Type	Physical domain
PD_A9_CPU	VDD_CPU	digital	Cortex-A9 platform
PD_A9_CPU0	VDD_CPU with toggle switch	digital	Cortex-A9 platform
PD_A9_CPU1	VDD_CPU with toggle switch	digital	Cortex-A9 platform
PD_A9_CPU2	VDD_CPU with toggle switch	digital	Cortex-A9 platform
PD_A9_CPU3	VDD_CPU with toggle switch	digital	Cortex-A9 platform
PD_SPARC_CPU	VDD_CPU with toggle switch	digital	SPARC platform
PD_VC810E	VDD_SOC with toggle switch	digital	VPU_Sub (VC810E)
PD_SOC	VDD_SOC	digital	NOC, Storage-Sub, Peri-Sub, Top
PD_SOC_MIPI	VDD_SOC	digital	SENS_Sub (MIPI DPHY)
PD_SOC_CMLK	VDD_SOC	digital	SENS_Sub (Camer Link PHY)
PD_SOC_PCIE	VDD_SOC	digital	HSIO_Sub (PCIe controller & PHY)
PD_SOC_GRIO	VDD_SOC	digital	HSIO_Sub (GRIO controller & PHY)
PD_SOC_DISP	VDD_SOC	digital	DISP_Sub (LVDS PHY)
PD_AI810	VDD_AI810	digital	AI810-OI
PD_DDR	VDD_DDR	digital	DDR controller & PHY
PD_RTC	VDD_RTC	digital	RTC Logic & Macro & IO
Analog_V0P8	VDDA_0P8	analog	Analog 0.8V
Analog_V1P8	VDDA_1P8	analog	Analog 1.8V

Analog_V2P5	VDDA_2P5	analog	Analog 2.5V
Analog_V3P3	VDDA_3P3	analog	USB2.0/SDEMMC PHY 3.3V
DRAM_IO	VDDIO_DRAM	IO	DRAM IO
PD_VDDIO18	VDDIO_1P8	IO	1.8V IO
PD_VDDIO33	VDDIO_3P3	IO	3.3V IO

6.3.6. Power-on/Power-off and power supply handshake

The external PMIC shall supply power to SoC according of the following sequences.

- Power-on sequence

The power-on sequence shall be implemented in the following order:

1. VDD_RTC;
2. VDDA_3P3_RTC;
3. VDDIO_3P3_RTC;
4. VDD_SOC and VDDA_0P8_XXX;
5. VDD_CPU and VDD_DDR (can be used with VDD U SOC);
6. VDDA_1P8_XXX;
7. VDDA_2P5_XXX and VDDA_3P3_XXX;
8. VDDIO_3P3, VDDIO_1P8 and VDDIO_DRAM;
9. RTC_RESETN released (should be asserted during VDDIO_3P3_RTC, VDD_RTC, and VDDA_3P3_RTC power-on, and remain asserted until the 32K XTAL clock is stable and the power rail has no order requirements);
10. -RTC_ISO_EN released (should be declared during the entire power-on process).

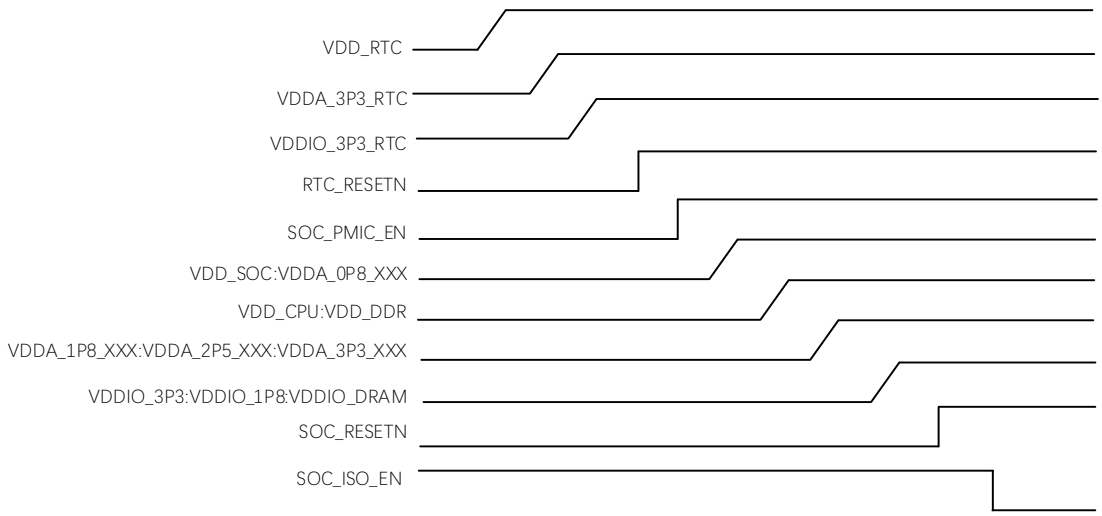

Figure 6-3 Yulong810A power-on sequence

When power-up, it recommends VDD_AI810 stay off to reduce the power during boot, and turned on by SW later. They can also be turned on together with VDD_SOC or any time after that.

During the chip power-up, the power of the PCIe PHY, GRIO PHY, MIPI PHY, CameraLink PHY and LVDS PHY should be off. After chip power-up, the power sequence of these PHYs should follow the requirement in the PHY specification.

- Power-off sequence

  The Soc power-off sequence shall be implemented in the following order:
  1. VDDIO_3P3, VDDIO_1P8 and VDDIO_DRAM.
  2. VDDA_1P8_XXX, VDDA_2P5_XXX and VDDA_3P3_XXX.
  3. VDD_SOC after turning off other power supplies (or turning off at the same time with other power supplies)
  4. VDDIO_3P3_RTC and VDDA_3P3_RTC
  5. VDD_RTC
  6. During power-off period, other power supplies have no power sequence.

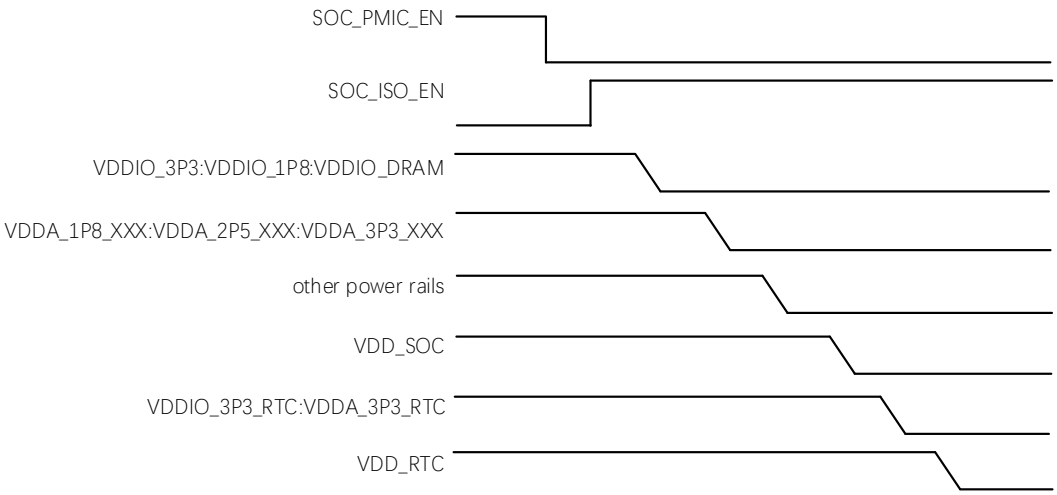

Figure 6-4 Yulong810A power-off sequence

- Power supply handshake sequence

External PMIC handshaking Yulong810A. Figure 4-6 shows handshake sequence between Yulong810A and PMIC. Yulong810A outputs SOC_PMIC_EN to PMIC and PMIC output SOC_ISO_EN to Yulong810A.

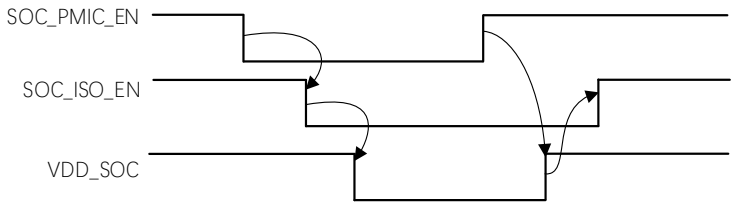

Figure 6-5 Yulong810A and PMIC timing

6.3.7. Power Management Unit (PMU)

Yulong810A integrates a PMU for SoC power management.

When the PMU receives a power-down/power-on request from the hardware/software, it will be isolated and the power switch will be enabled for power control. After the PMU completes power control, a confirmation will be returned to the requester.

In addition to the power control of the normal power mode conversion, the hardware power request in Yulong810A will include the eFuse configuration whether these blocks are implemented when the SoC is used in different scenarios.

6.3.8. RTC

RTC power supply and power on and off mode The RTC power supply mode of Yulong810A chip is as follows:

- When the SOC is powered off, use a 3V rechargeable button battery to power the RTC;
- When the SOC is powered off, use a voltage conversion device such as LDO in the PCB or chip to convert the 3V of the button battery into 1.8V and 1.0V for the on-chip 32K oscillator and RTC respectively;
- When the power module of the PCB board is powered off and the RTC is powered by a button battery, only the calendar function of the RTC can be used, and the RTC cannot be used to wake up the SOC;
- The RTC calendar accuracy is affected by various factors such as 32.768Khz passive crystal temperature and board-level noise;
- When the SOC is powered off, but the PCB board power module is not powered on, the RTC power domain is powered by the PCB board power module. At this time, the timing function of RTC can be used to wake up the SOC.

6.3.9. Boot

The ARM and SPARC processor of the Yulong810A chip can choose to use the direct external interface EXTERN BUS FLASH or the internal BOOT program to boot. Selection of boot method is determined by the remap pin level(SPARC_BOOT_REMAP for SPARC, BOOT_SEL2 for ARM) of the Yulong810A startup configuration pin when the SoC is powered on.

ARM supports SPI/NOR/NAND/EMMC/SD FLASH and SPARC supports SPI/NOR/NAND FLASH to store startup applications or use serial KERMIT protocol to download startup applications. The above selection method is determined by the configuration of BOOT_2ND[0-6].

ARM internal BOOTROM program is hardwired at 0XFFFF0000 address. SPARC internal BOOTROM program is hardwired at 0XC1000000 address.

BOOT supports DEBUG mode.
When the corresponding DEBUG mode pin BOOT_2ND[7] is set to 1, BOOT will output the running status from the serial port (ARM uses serial port 0, SPARC use SPARC special serial port).

The internal BOOT program mainly provides the following functions:
1. FLASH storage data supports verification and inspection, which can identify and skip invalid error data.
2. Multiple storage backup data in FLASH.
3. According to FLASH settings, some simple processor read-write control can be performed.
4. It can copy FLASH storage data to the designated memory, and the processor jumps to the designated address to run the function.

The contents of the internal BOOTROM program copy and start FLASH have specific format requirements. Orbita provides relevant FLASH storage format conversion software, which can easily generate FLASH binary programming files. The serial communication frequency under 24MHz crystal oscillator frequency is 115200, and the access speed of EMI interface storage setting is 1MHz. Other interface rates can be selected according to the setting of BOOT_2ND[4].

Table 6-9 Selection list of internal BOOT and external EMI startup methods

REMAP signal	BOOT_2ND[0:7]	Description
0	Control the working mode of internal BOOT program	The processor fetches instructions from the internal BOOTROM to run the internal BOOT program. The internal BOOT program will select to enter the FLASH boot mode, serial port mode or debug mode according to the BOOT2ND pin configuration.
1	REMAP bit 1 is the related pin function is ignored	The processor fetches instructions from the 16-bit parallel interface memory 0 address of the EMI interface to run.

Table 6-10 Selection of internal BOOT startup mode

<table>
<tr><th>BOOT_2ND[7]</th><th>BOOT_2ND[6]</th><th>BOOT_2ND[5:3]</th><th>BOOT_2ND[2:0]</th></tr>
<tr><td rowspan="2">When this bit is 1, the DEBUG mode is turned on, and the BOOTROM program will output the current BOOTROM running status as a character string.
When this bit is 0, the DEBUG mode is closed, and the BOOTROM program outputs status information.</td><td>1: system set to: NAND FLASH boot mode</td><td>NANDFLASH block size configuration:
000: 32 pages per block
001: 64 pages per block
010: 128 pages per block
011: 256 pages per block
100: 512 pages per block
101: 1024 pages per block
110: 2048 pages per block
110: 4096 pages per block</td><td>NANDFLASH page size configuration:
001: 2048 bytes per page
010: 4096 bytes per page
011: 8192 bytes per page
Other values: does not support other page size FLASH startup methods.</td></tr>
<tr><td>0: system set to: non-NAND FLASH boot mode</td><td>Some interfaces can adjust the interface rate through this setting, and the interface rate of the external crystal oscillator frequency will change proportionally.

UART rate and EMI rate will not change, fixed 24M crystal oscillator rate,
UART rate: 115200,
EMI rate: 1M.

010: Turn on ARM CACHE to increase operating speed

000: Set to low-speed mode (QSPI rate: 6M, SD/MMC rate: 300K/3M);

001: Set to high-speed mode (QSPI rate: 12M, SD rate: 400K/4M).</td><td>000: QSPI NOR FLASH start
001: ARM SD boot
010: ARM EMMC card starts
011: Serial command download start
100: EMI interface 16-bit parallel interface start
101: EMI interface 8-bit parallel interface start

Other values:
Enter the wait mode. The processor enters a while loop and waits for the emulator to connect. If there is an error in the storage space in this mode, the processor will be reset by the watchdog, which can easily cause the problem of the emulator not being connected.</td></tr>
</table>