VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY

VDMR16M08XS44XX1V35 USER MANUAL

Version : A1

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VDIC-MRAM

HIGH-SPEED 3.3V 2M × 8bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1 DESCRIPTION

The VDMR16M08XS44XX1V35 is a 1 x 16,777,216-bit Magnetoresistive Random Access Memory device. Manufactured with VDIC Very Dense SiP technology, this device stacks 16-Mbit MRAM dies. It is organized as one independent dies of 2M x 8bit wide data interface.

The VDMR16M08XS44XX1V35 offers SRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR16M08XS44XX1V35 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The VDMR16M08XS44XX1V35 has one die. It can be selected with dedicated #E. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

2 FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM
- Stack of one16Mbit MRAM
- Organized as 1 die of 2M x 8 bit memory
- One independent Ship Select
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Automotive Temperatures
- 44-lead SOP package

3 BLOCK DIAGRAM

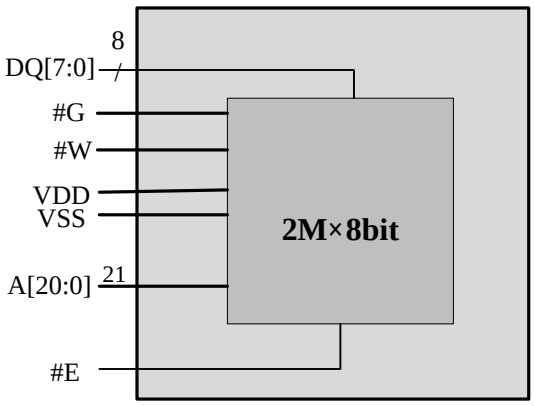

Figure 1 Block diagram

4 PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
DC	1	44	**DC**
A20	2	43	**A19**
A0	3	42	**DC**
A1	4	41	**A18**
A2	5	40	**A17**
A3	6	39	**A16**
A4	7	38	**A15**
#E	8	37	**#G**
DQ0	9	36	**DQ7**
DQ1	10	35	**DQ6**
VDD	11	34	**VSS**
VSS	12	33	**VDD**
DQ2	13	32	**DQ5**
DQ3	14	31	**DQ4**
#W	15	30	**DC**
A5	16	29	**A14**
A6	17	28	**A13**
A7	18	27	**A12**
A8	19	26	**A11**
A9	20	25	**A10**
DC	21	24	**DC**
DC	22	23	**DC**

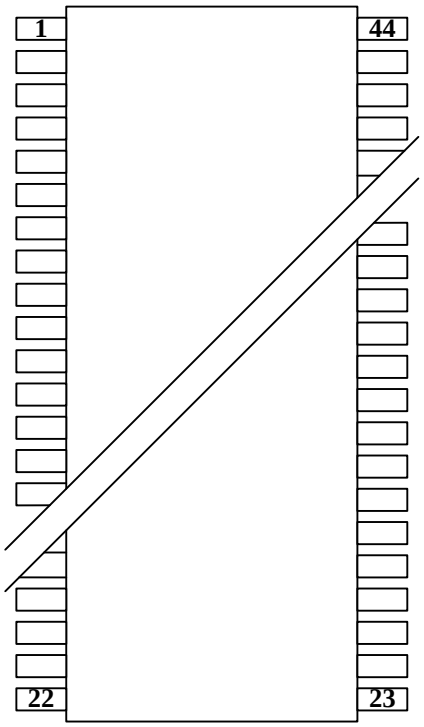

Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#E	Chip Enable	Disables or enables memory operation
A0 ~ A20	Address	21-bit addresses

#W	Write enable	Enables write operation common to all memory dies
#G	Output enable	Enables data output common to all memory dies
DQ0~ DQ7	Data input/output	Data inputs/outputs 8-bit wide bus
VDD/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.
DC	Do not connect	These pins do not connect

5 ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 ~ 4.0	V
Voltage on any pin relative to V_{SS}	V_{IN}	-0.5 ~ V_{DD}+0.5	V
Output current per pin	I_{OUT}	±20	mA
Operating Temperature Range	T_{OPR}	-45~ +95	℃
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	0.6	W

5.2 RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input logic high voltage	V_{IH}	2.2	--	V_{DD}+0.3	V
Input logic low voltage	V_{IL}	-0.5	--	0.8	V

5.3 DC CHARACTERISTICS

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	I_{OL}= +4mA	——	0.4	V
Output voltage high level	V_{OH}	I_{OL}= -4mA	2.4	——	V

6 TYPICAL APPLICATION

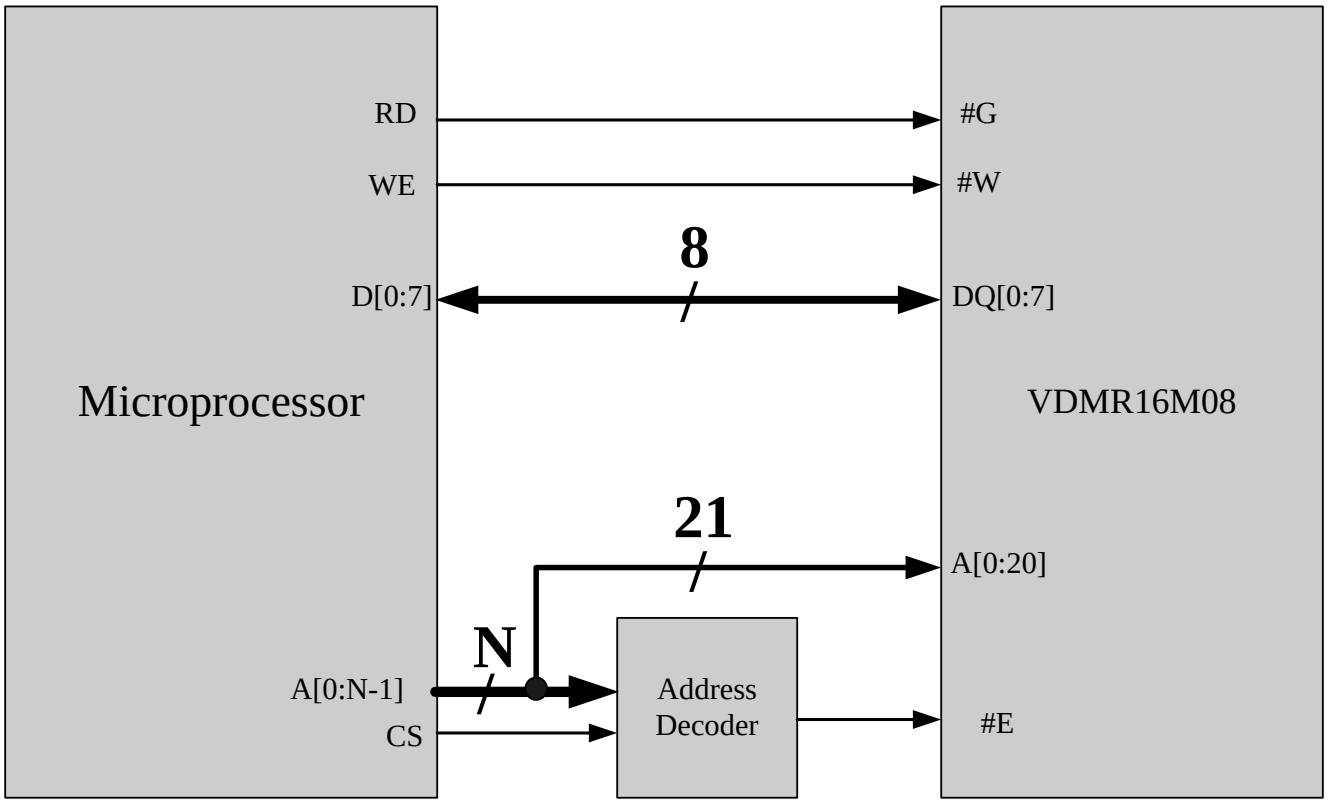

Figure 3 Typical application

7 ORDERING INFORMATION

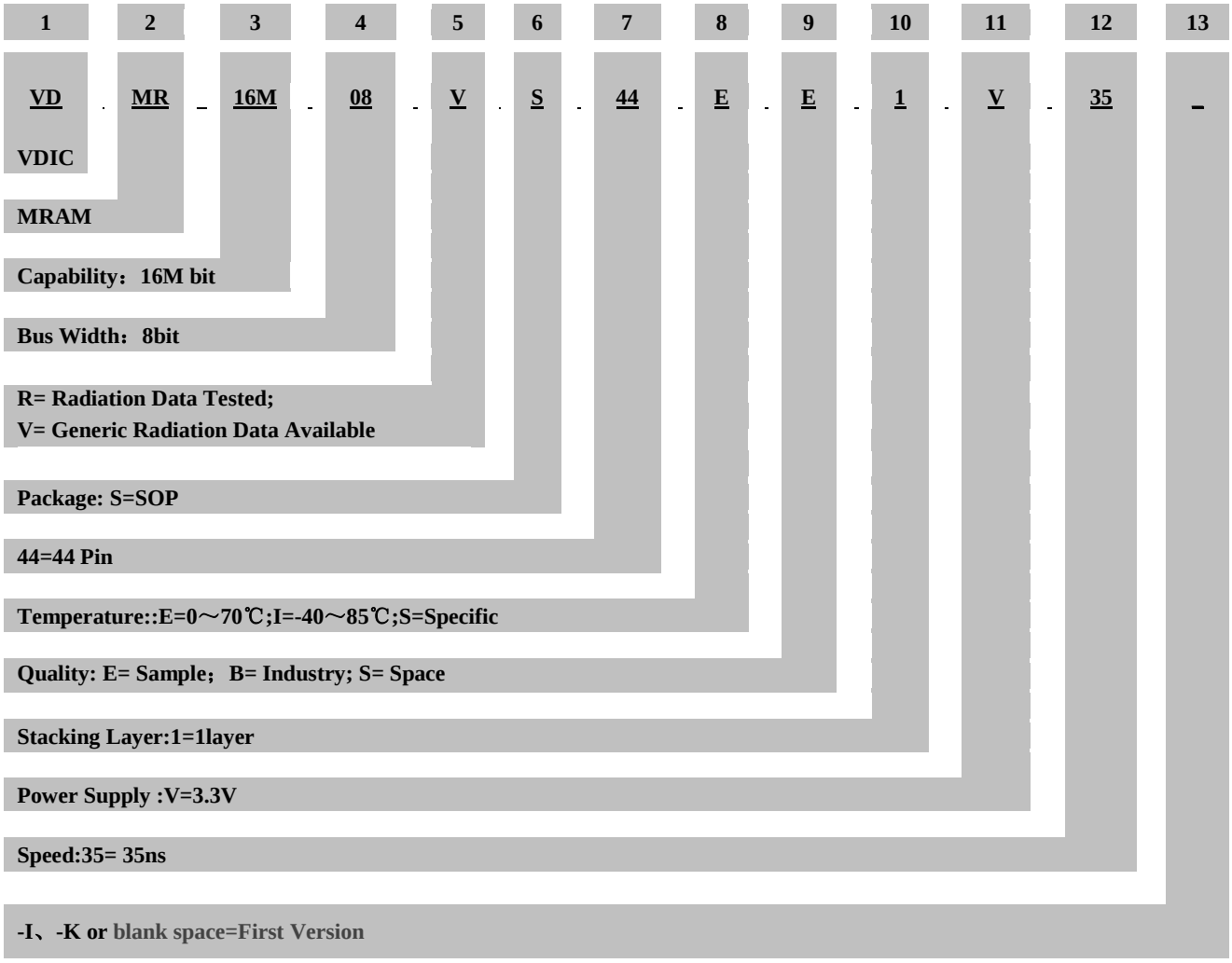

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDMR16M08VS44EE1V35	16M	8	-	-	-	SOP44	0 ~ +70
VDMR16M08VS44IB1V35	16M	8	-	-	-	SOP44	-40 ~ +85
VDMR16M08RS44SS1V35	16M	8	>60	<40	>37	SOP44	-45 ~ +95

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 PACKAGE DIMENSIONS

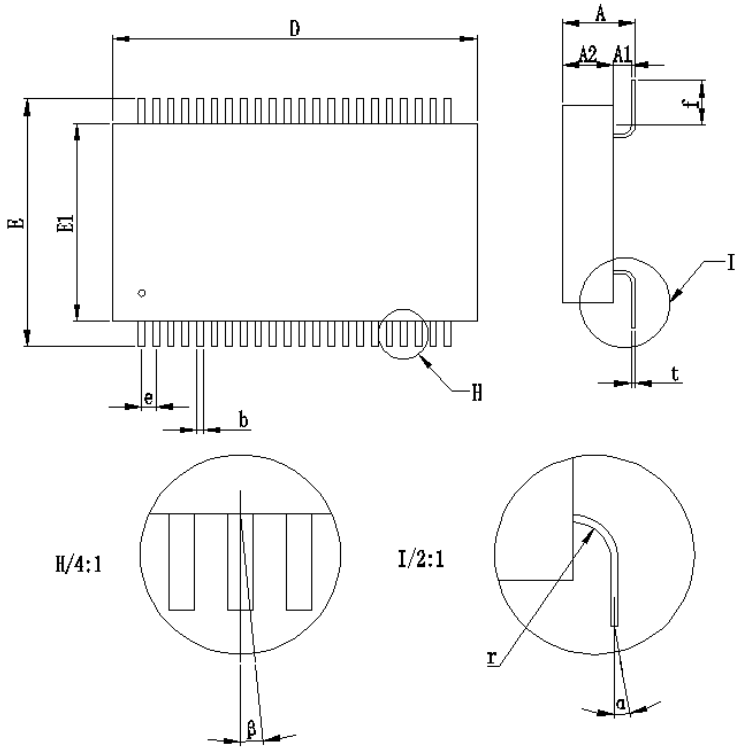

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	3.70	4.40
A2	2.50	3.10
D	19.80	20.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	

NOTE：1. Unit：mm

2. A1= A - A2

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 1,2017	First Created
A1	May 22, 2018	Modified Operating Temperature Range and Storage temperature.