

VDIC EEPROM

VDEE5M40XS64XX5V250 USER MANUAL

Version : A5

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Contents

1	Description	1
2	Features	1
3	Block Diagram	2
4	Pin Configurations.....	3
5	Command Operation	4
5.1	Absolute Maximum Ratings.....	4
5.2	Recommended DC Operating Conditions.....	4
5.3	DC Characteristics (VCC =2.7V to 3.6 V)	4
6	Typical Application.....	5
7	Ordering Information.....	6
8	Package Dimensions.....	7
9	REVISION HISTORY	8

VDIC-EEROM

3.3V 128K x 40bit

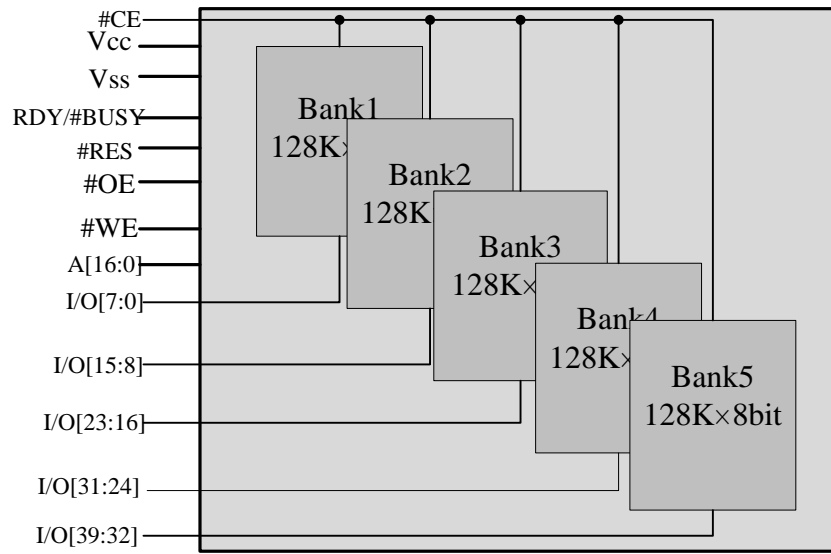
1 Description

The VDEE5M40XS64XX5V250 is a 131,072 words of 40bits Electrically Erasable and Programmable CMOS ROM. It is organized as 5 dies of 1Mbit. Each die has 8-bit interface and is selected with specific #CE. All other signals are common to the five EEPROM 1Mbit. The device is manufactured using well known SIP technology. It is particularly well suited for use in high reliability, high performance and high density system applications. The VDEE5M40XS64XX5V250 is packaged in a 64 pins SOP.

2 Features

- Single 3.3 V supply: 2.7 V to 3.6 V
- Access time: 250 ns (max)
- Power dissipation
 - Active: 100 mW/MHz, (max)
 - Standby: 550 μ W (max)
- On-chip latches: address, data, #CE, #OE, #WE
- Automatic byte write: 15 ms (max)
- Automatic page write (128 bytes): 15 ms (max)
- Data polling and RDY/#Busy
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4 erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by #RES pin

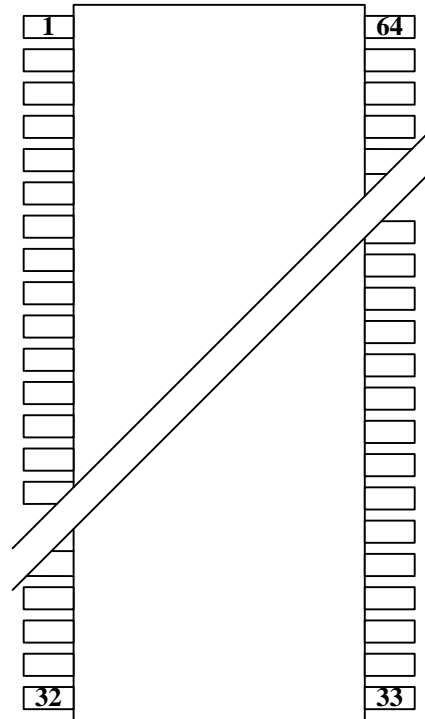
3 Block Diagram



(All other signals are common to the five memories)

4 Pin Configurations

Pin Id	Pin #		Pin Id
A11	1	64	I/O24
A9	2	63	I/O16
A8	3	62	I/O8
A4	4	61	I/O0
A5	5	60	I/O25
A6	6	59	I/O17
A7	7	58	I/O9
A12	8	57	I/O1
A14	9	56	I/O26
A16	10	55	I/O18
RDY/#BUSY	11	54	I/O10
VCC	12	53	I/O2
I/O32	13	52	I/O27
I/O33	14	51	I/O19
I/O34	15	50	I/O11
A15	16	49	I/O3
#RES	17	48	I/O28
#WE	18	47	I/O20
A13	19	46	I/O12
A0	20	45	I/O4
A1	21	44	I/O29
A2	22	43	I/O21
A3	23	42	I/O13
VSS	24	41	I/O5
I/O35	25	40	I/O30
I/O36	26	39	I/O22
I/O37	27	38	I/O14
I/O38	28	37	I/O6
#CE	29	36	I/O31
I/O39	30	35	I/O23
A10	31	34	I/O15
#OE	32	33	I/O7



Pin Descriptions

Name	Function
A0~A16	Address Input..
I/O0- I/O39	Data Input/Output Ports. 40 bit-directional ports are used to read data from or write data into the EEPROM.
#CE	Die Enable Input .When #CE is Low, the command input cycle becomes valid. When #CEn is High, all inputs are ignored.
RDY/#BUSY	Ready busy.
#RES	Reset input.

#OE	Output enable.
#WE	Write Enable Input. Enables write operation.
VCC	Power supply, connect to 3.3V
VSS	Ground

5 Command Operation

5.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage relative to V _{SS}	V _{CC}	-0.6 to +7.0	V
Input voltage relative to V _{SS}	V _{IN}	-0.5 to +7.0	V
Operating temperature range	T _{OPR}	-55 to +125	°C
Storage temperature range	T _{STG}	-65 to +150	°C
Power Dissipation	P _D	1	W

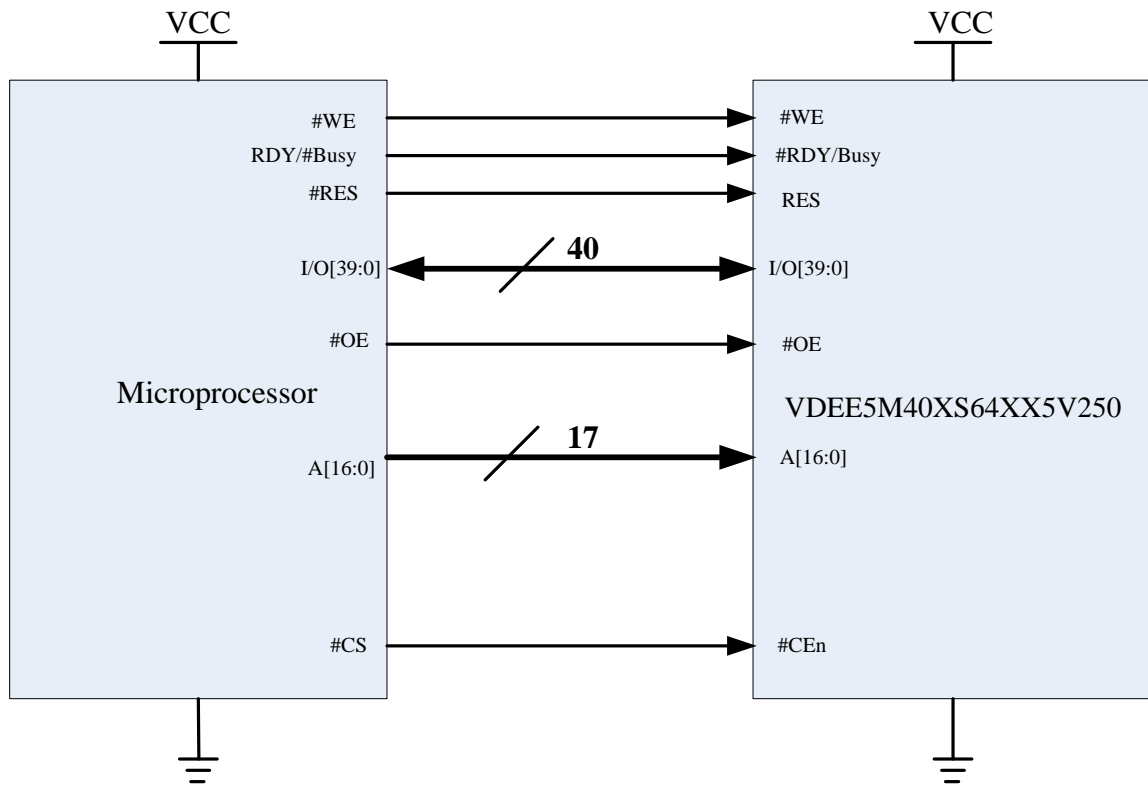
5.2 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.3	3.6	V
	V _{SS}	0	0	0	V
Input voltage	V _{IL}	-0.3	-	0.8	V
	V _{IH}	1.9	-	V _{CC} +0.3	V
	V _H	V _{CC} -0.5	-	V _{CC} +1.0	V

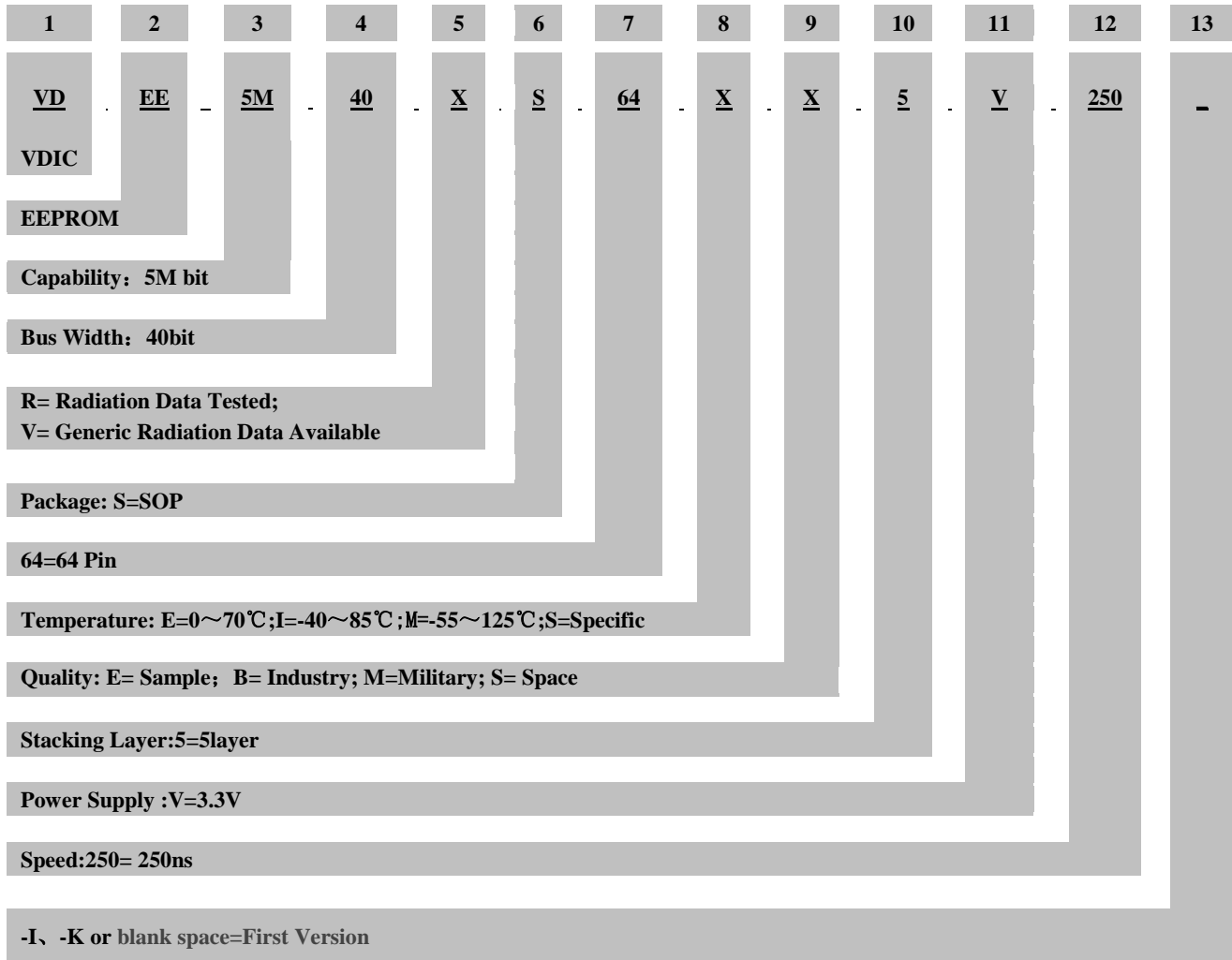
5.3 DC Characteristics (VCC =2.7V to 3.6 V)

Parameter	Symbol	Test conditions	min.	max.	Unit
Output voltage low level	VOL	V _{CC} =2.7V , I _{OL} = 2.1mA	—	0.4	V
Output voltage high level	VOH	V _{CC} =2.7V , I _{OH} = -400uA	2.16	—	V

6 Typical Application



7 Ordering Information



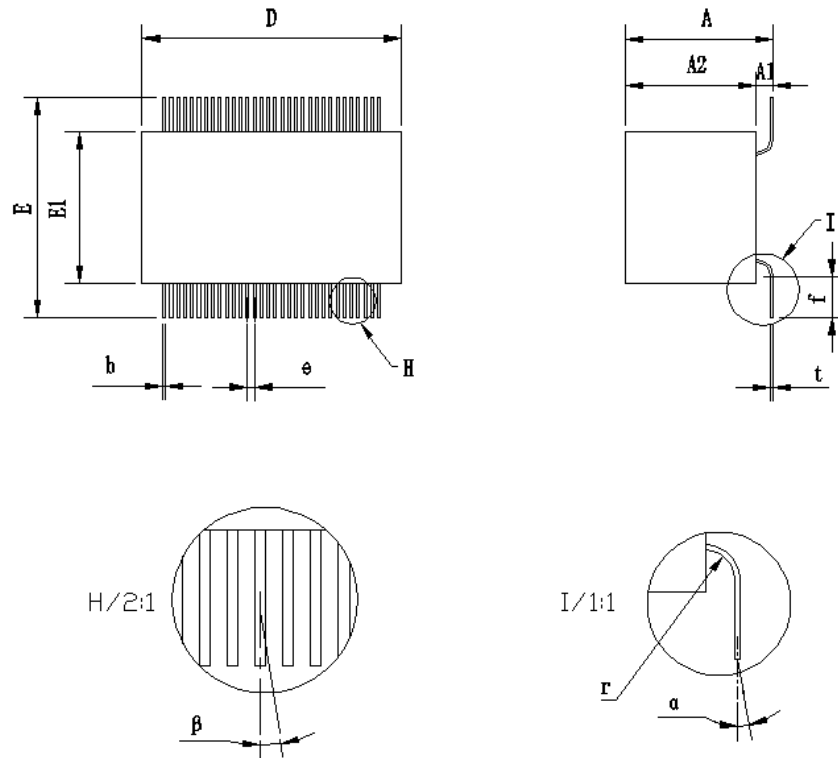
Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDEE5M40VS64EE5V250	5M	40	-	-	-	SOP64	0 ~ +70
VDEE5M40VS64IB5V250	5M	40	-	-	-	SOP64	-40 ~ +85
VDEE5M40VS64MB5V250	5M	40	-	-	-	SOP64	-55 ~ +125
VDEE5M40VS64MM5V250	5M	40	-	-	-	SOP64	-55 ~ +125
VDEE5M40RS64MS5V250	5M	40	30	99.8	25	SOP64	-55 ~ +125

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8 Package Dimensions



	Min	Max
A	10.40	11.10
A2	9.20	9.80
D	18.50	18.90
E	15.80	16.20
E1	10.80	11.20
f	3.00	
b	0.25	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE : 1.U int : mm		

2. A1= A - A2

9 REVISION HISTORY

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Mar 16,2018	Add or reduce chapters