# VDIC
# LOW-VOLTAGE
# DIFFERENTIAL SIGNALING
# DRIVER

# VDLV000108XS34XX1V01-31
# USER MANUAL

**Version: A2**

**Document NO.：ORBITA/SIP- VDLV000108XS34XX1V01-31-USM-01**
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# VDLV- Low-voltage differential signal Driver

# 3.3V Eight Line Drivers, based on Quad

## 1 Description

The VDLV000108XS34XX1V01-31 is Eight CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The VDLV000108XS34XX1V01-31 accepts LVTTL/LVCMOS input levels and translates them to low voltage (450 mV) differential output signals.

The VDLV000108XS34XX1V01-31 provides a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

## 2 Features

- >400Mbps (200MHz) switching rates
- ±450 mV differential signaling
- 3.3V power supply
- Ultra low power dissipation
- 0.6 ns maximum differential skew
- 4.5ns maximum propagation delay
- Compatible with IEEE1596.3SCILVDS standard
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Cold sparing all I/O pins
- Variable Temperature range

  0℃ to 70℃

  -40℃ to +85℃

  -55℃ to +125
- Available screening option for high reliability application

# 3 Block Diagram

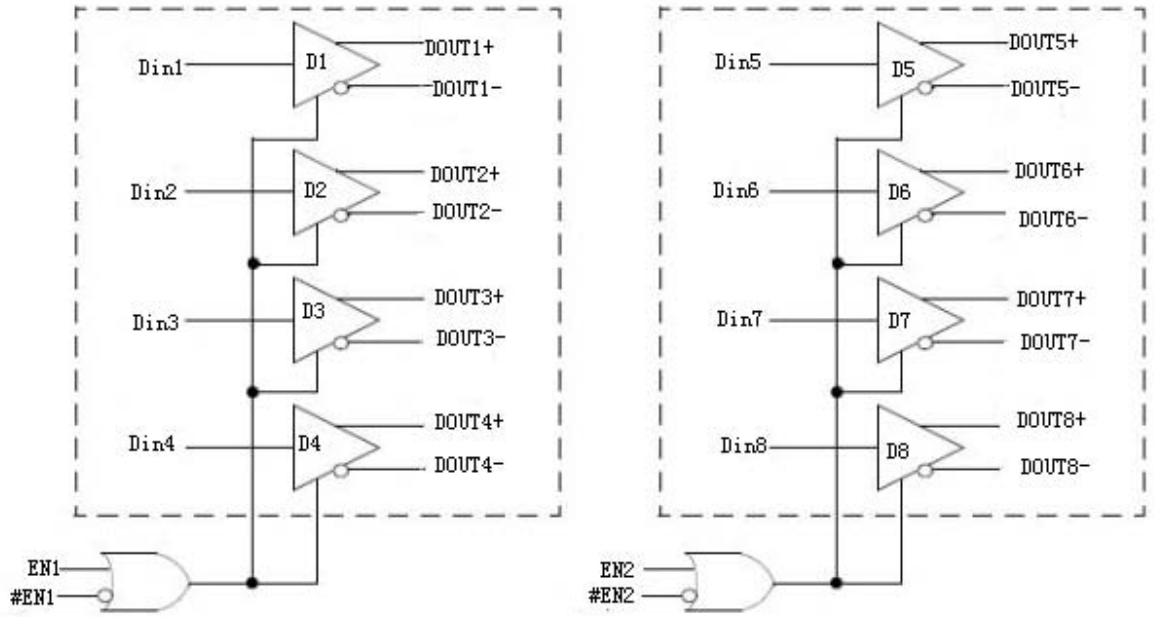



Figure 1 Block Diagram

# 4 Pin Descriptions

| Pin Id | Pin # | | Pin Id |
|---|---|---|---|
| Din1 | 1 | 34 | Vdd |
| Dout1+ | 2 | 33 | Din4 |
| Dout1- | 3 | 32 | Dout4+ |
| EN1 | 4 | 31 | Dout4- |
| Dout2- | 5 | 30 | #EN1 |
| Dout2+ | 6 | 29 | Dout3- |
| Din2 | 7 | 28 | Dout3+ |
| GND | 8 | 27 | Din3 |
| GND | 9 | 26 | Vdd |
| Din5 | 10 | 25 | Vdd |
| Dout5+ | 11 | 24 | Din8 |
| Dout5- | 12 | 23 | Dout8+ |
| EN2 | 13 | 22 | Dout8- |
| Dout6- | 14 | 21 | #EN2 |
| Dout6+ | 15 | 20 | Dout7- |
| Din6 | 16 | 19 | Dout7+ |
| GND | 17 | 18 | Din7 |

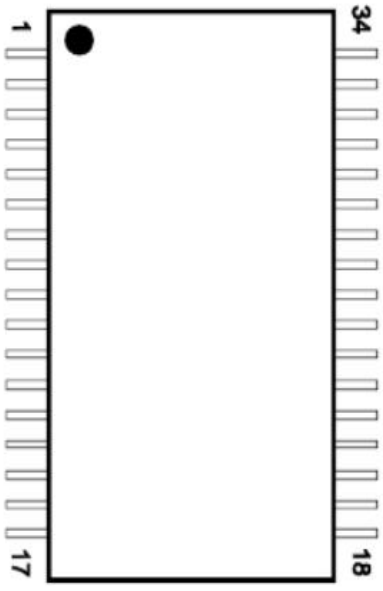



Figure 2 Pin Configuration

Table 1 Pin Description

| Pin Name | Function |
|---|---|
| EN1 ~ EN2 | Enable(HI=ENABLE) |
| #EN1 ~ #EN2 | Enable(LO=ENABLE) |
| Din1 ~ Din8 | LVTTL input signal |
| Dout1+ ~ Dout8+ | Differential(LVDS) non-inverting output |
| Dout1- ~ Dout8- | Differential(LVDS) inverting output |
| $V_{DD}$ | Supply Voltage(3.0-3.6V) |
| GND | Ground |

# 5 Electrical Specifications

## 5.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

| Characteristics | Symbol | Maximum ratings | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 ~ +4.0 | V |
| Input Voltage(Din) | $V_{IN}$ | -0.5 ~ VCC +0.5 | V |
| Operating Temperature Range | $T_{OPR}$ | -55 ~ +125 | ℃ |
| Storage Temperature Range | $T_{STG}$ | -65 ~ +150 | ℃ |

## 5.2. Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

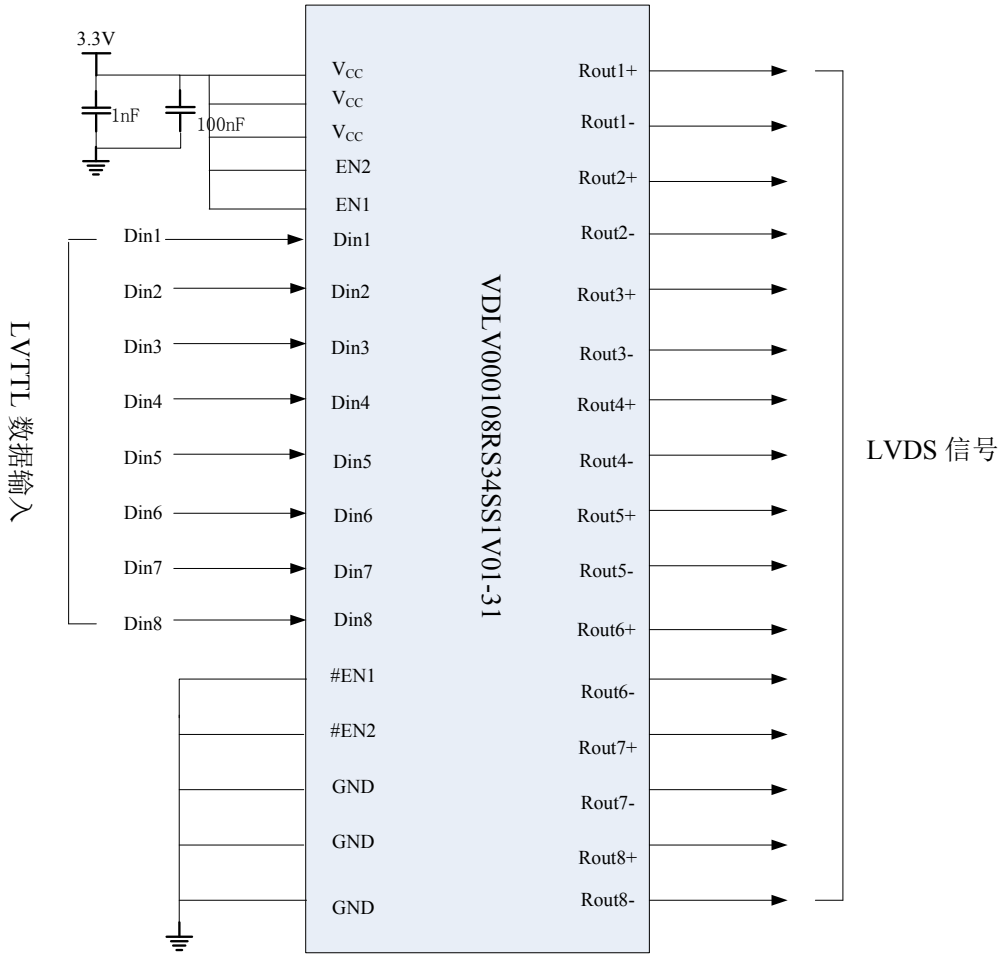
| Parameter | Symbol | Min | $T_{YP}$ | Max | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.3 | 3.6 | V |
| Input high voltage | $V_{IH}$ | 2.0 | —— | 3.6 | V |
| Input low voltage | $V_{IL}$ | 0 | —— | 0.8 | V |

## 5.3. DC Characteristics

Table 4 DC Characteristics

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Differential output voltage Magnitude | $V_{OD}$ | 247 | 454 | mV |
| Offset Voltage | Vos | 1.125 | 1.375 | V |

# 6 Typical Application




**注意:在LVDS信号接收器的输入端通常需接100Ω的终端电阻**

Figure 3 Typical Application

# 7 Ordering Information

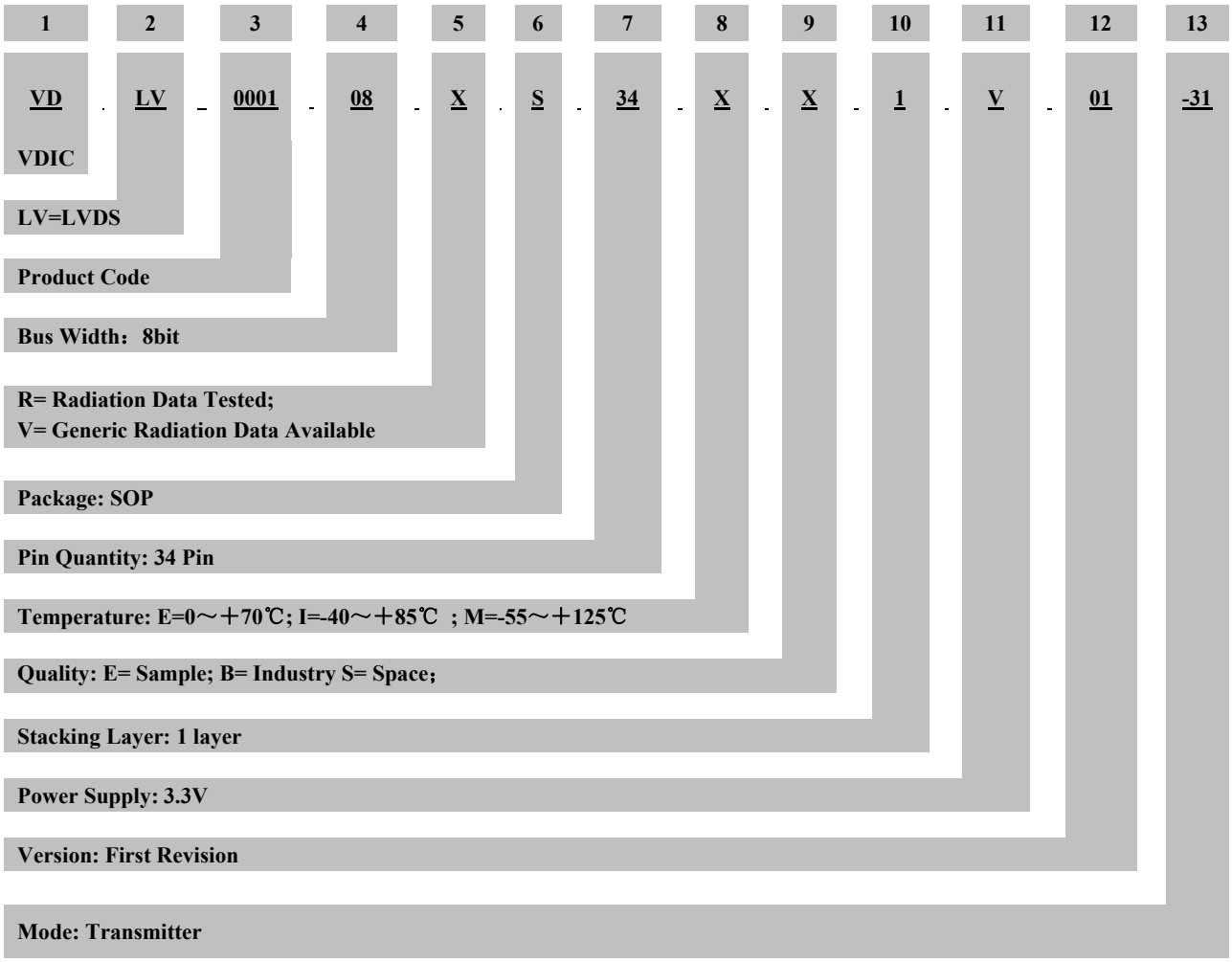



Table 5 Ordering Information

| Bank Number | Bus Width (bit) | Radiation | | | Packaging | Temperature (℃) |
|---|---|---|---|---|---|---|
| | | TID[1] | SEL[2] | SEU[3] | | |
| VDLV000108VS34EE1V01-31 | 08 | -- | | | SOP34 | 0～+70 |
| VDLV000108VS34IB1V01-31 | 08 | -- | | | SOP34 | -40～+85 |
| VDLV000108VS34MM1V01-31 | 08 | -- | | | SOP34 | -55～＋125℃ |
| VDLV000108RS34MS1V01-31 | 08 | 100（TBD，25℃） | 80（TBD，25℃） | 31（TBD，25℃） | SOP34 | -55～＋125℃ |

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（MeV.cm$^2$/mg）
[3] SEU:SEU Threshold （MeV.cm$^2$/mg）

# 8 Package Dimensions

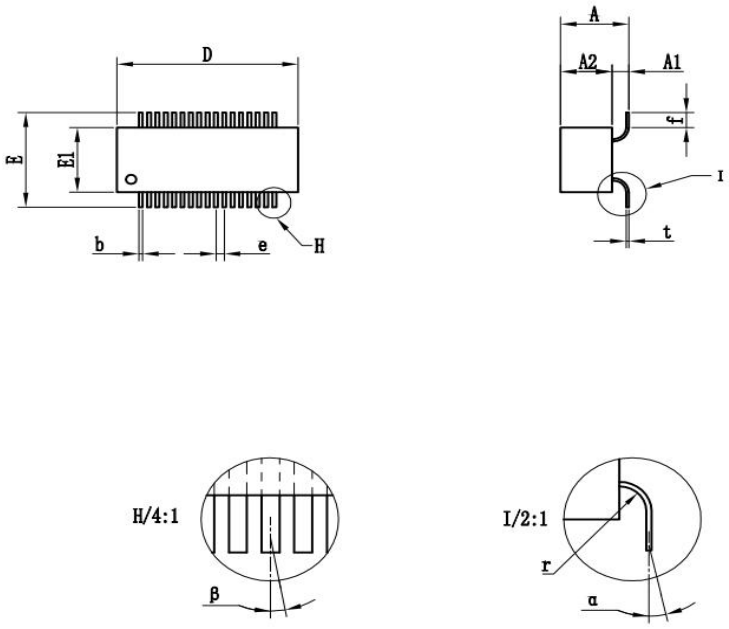



Figure 4 Package Dimensions

Table 6 Dimensions Information

| | Min | Max |
|---|---|---|
| A | 3.7 | 4.4 |
| A2 | 2.5 | 3.1 |
| D | 13.9 | 14.3 |
| E | 7.8 | 8.2 |
| E1 | 5.3 | 5.7 |
| f | 1.30 | |
| b | 0.3 | |
| e | 0.65 | |
| r | 1.00 | |
| t | 0.20 | |
| α | ≤3° | |
| β | ≤3° | |
| NOTE：1. Unit：mm<br>2. A1= A - A2 | | |

# 9 Pads Designation

It is highly recommended to design pads as below.

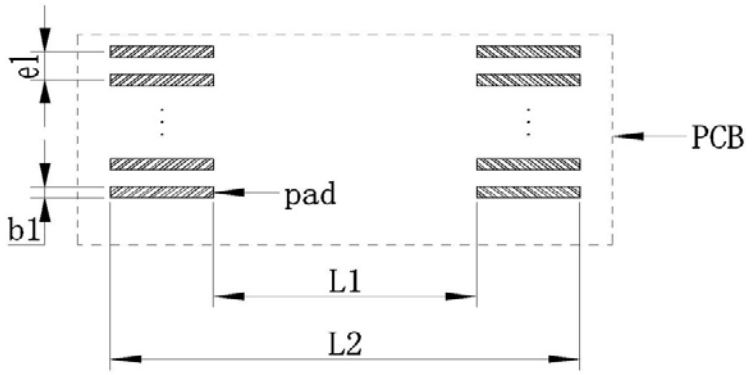



Figure 5 Pads Dimensions

NOTE:

e1: 0.65 mm;

b1: 0.45 mm;

L1: 2.2 mm;

L2: 9.2 mm

# 10 Revision History

Table 7 Revision History

| Revision | Date | Description of Change |
|---|---|---|
| A0 | Mar 15, 2018 | Initial Release |
| A1 | Mar 25, 2020 | Update operating temperature range |
| A2 | July 16, 2021 | Add pads designation and radiation |