VDIC DDR2 SYNCHRONOUS DYNAMIC RAM

VD2D4G72XB191XX3U6 USER MANUAL

Version : B1

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VDIC-DDR2 SDRAM

HIGH-SPEED 1.8V 64M x 72bit

SYNCHRONOUS DYNAMIC RAM

1. DESCRIPTION

The VD2D4G72XB191XX3U6 is a 4Gbit DDR2 SDRAM high-density System-in-Package memory module. It is organized with 5 chips, of which 4 4Gbit(64Mx16bit) chips form 64bit and 1 chip is used as 8-bit ECC. The three-dimensional packaging technology is used to interconnect the multi-layer memory circuits to form a high-density DDR2 memory module with high reliability, high stability and miniaturization. It is particularly well suited for use in high reliability, high performance and high density system applications, such as servers or workstations.

2. FEATURES

- Organized as 64Mx72bit
- Clock frequency up to 333MHz
- VCC= 1.8V ± 0.1V
- SSTL_18 interface
- 8 internal banks for concurrent operation
- 4-bit prefetch architecture
- Programmable CAS Latency: 3, 4, 5, 6 and 7
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6
- Write Latency = Read Latency-1
- Programmable Burst Sequence: Sequential or Interleave
- Programmable Burst Length: 4 and 8
- Automatic and Controlled Precharge Command
- Power Down Mode
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8 us (8192 cycles/64 ms)
- ODT (On-Die Termination)
- Weak Strength Data-Output Driver Option
- Bidirectional differential Data Strobe
- On-Chip DLL aligns DQ and DQs transitions with CK transitions
- DQS# can be disabled for single-ended data strobe
- Differential clock inputs CK and CK#
- PASR (Partial Array Self Refresh)
- Package:BGA191
- Operating temperature:
  - ■ 0℃~+70℃
  - ■ -40℃~+85℃
  - ■ -40℃~+105℃

3. BLOCK DIAGRAM

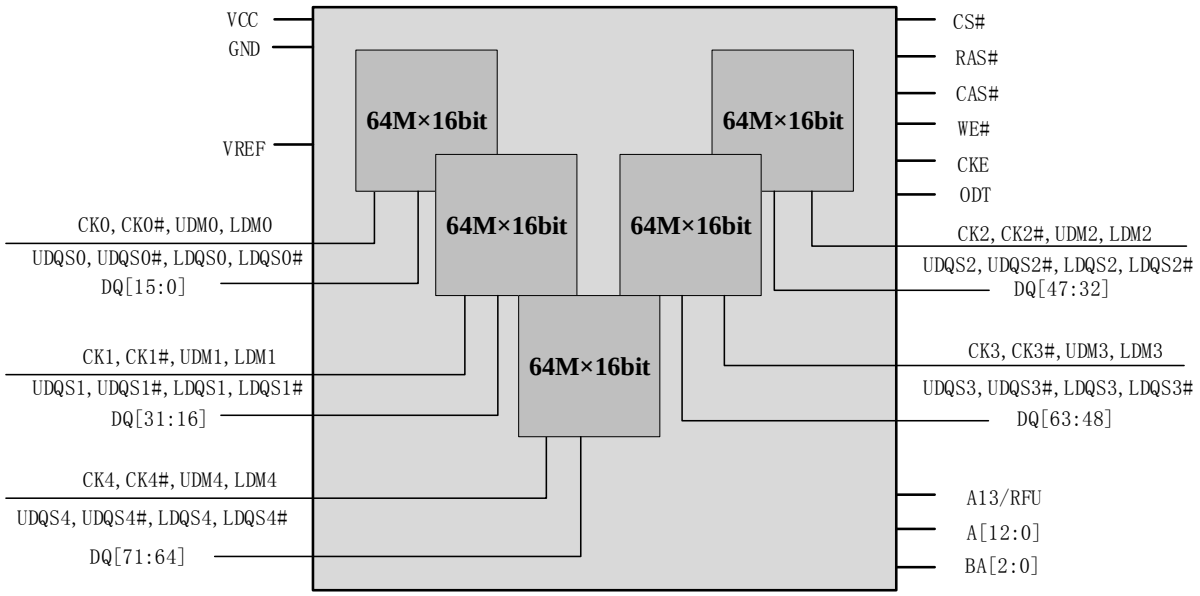

Figure-1 Block diagram

4. PIN DESCRIPTIONS

Table-1 Pin List

Pin Id	Pin#			Pin Id	Pin Id	Pin#			Pin Id
	A1		E1	DQ60	NC	L1		U1	DQ26
CK3#	A2		E2	GND	A9	L2		U2	LDQS1
UDQS3#	A3		E3	DQ59	A10	L3		U3	DQ27
VCC	A4		E4	DQ54	GND	L4		U4	DQ20
NC	A5		E9	VCC	NC	L9		U5	LDQS4#
NC	A6		E10	UDQS2	GND	L10		U6	DQ67
VREF	A7		E11	UDQS2#	BA0	L11		U7	GND
DQ35	A8		E12	NC	WE#	L12		U8	UDM0
DQ44	A9		F1	NC	CK1#	M1		U9	DQ15
VCC	A10		F2	ODT	CK1	M2		U10	NC
LDM2	A11		F3	DQ62	UDQS4	M3		U11	LDM0
CK2#	A12		F4	DQ57	UDQS4#	M4		U12	DQ3
CK3	B1		F9	GND	CK4#	M9		V1	LDQS1#
DQ58	B2		F10	DQ47	NC	M10		V2	DQ16
UDQS3	B3		F11	DQ45	NC	M11		V3	DQ22
DQ61	B4		F12	DQ39	NC	M12		V4	DQ69

Pin Id	Pin#			Pin Id	Pin Id	Pin#			Pin Id
LDQS3#	B5		G1	NC	NC	N1		V5	LDQS4
DQ50	B6		G2	A8	NC	N2		V6	NC
GND	B7		G3	A4	DQ21	N3		V7	DQ70
DQ33	B8		G4	GND	DQ23	N4		V8	DQ0
DQ41	B9		G9	NC	CK4	N9		V9	LDQS0#
DQ46	B10		G10	DQ37	LDM4	N10		V10	UDQS0#
DQ34	B11		G11	GND	UDM4	N11		V11	UDQS0
CK2	B12		G12	A13/RFU	GND	N12		V12	CK0
NC	C1		H1	NC	VCC	P1		W1	DQ18
UDM3	C2		H2	A0	NC	P2		W2	DQ25
LDM3	C3		H3	VCC	DQ29	P3		W3	DQ19
NC	C4		H4	CS#	DQ31	P4		W4	DQ71
LDQS3	C5		H9	GND	NC	P9		W5	VREF
DQ48	C6		H10	CAS#	NC	P10		W6	DQ66
DQ53	C7		H11	CKE	DQ14	P11		W7	DQ68
DQ38	C8		H12	BA1	DQ9	P12		W8	DQ5
GND	C9		J1	NC	LDM1	R1		W9	LDQS0
UDM2	C10		J2	RAS#	UDM1	R2		W10	DQ13
LDQS2	C11		J3	A2	UDQS1#	R3		W11	GND
DQ32	C12		J4	A6	UDQS1	R4		W12	CK0#
DQ52	D1		J9	VCC	DQ1	R9		Y1	VCC
DQ51	D2		J10	A1	DQ12	R10		Y2	DQ28
DQ49	D3		J11	A5	DQ11	R11		Y3	DQ17
DQ63	D4		J12	VCC	DQ6	R12		Y4	GND
DQ56	D5		K1	NC	NC	T1		Y5	DQ64
DQ55	D6		K2	BA2	DQ24	T2		Y6	NC
DQ36	D7		K3	A11	GND	T3		Y7	DQ65
DQ43	D8		K4	GND	DQ30	T4		Y8	GND
DQ42	D9		K9	NC	NC	T9		Y9	DQ2
DQ40	D10		K10	A3	DQ10	T10		Y10	DQ7
LDQS2#	D11		K11	A12	DQ4	T11		Y11	VCC
VCC	D12		K12	A7	VCC	T12		Y12	DQ8

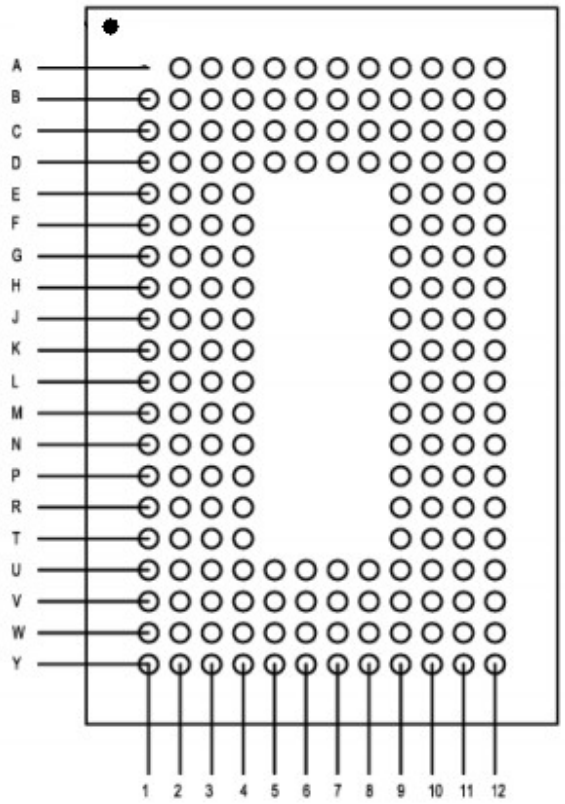

Figure-2 Top View

Table-2 Pin Description

Symbol	Description
CK0~CK4, CK0#~CK4#	Input clocks.
CKE	Clock enable.
CS#	Chip Select.
RAS#,CAS#,WE#	Command control inputs.
A[12:0]	Address
A13/RFU	Reserved For Future Use,as an NC pin inside the memory module.
BA[2:0]	Bank Address.
DQ[71:0]	I/O.
UDQS0~UDQS4, UDQS0#~UDQS4#	Upper Byte Data Strobe.
LDQS0~LDQS4, LDQS0#~LDQS4#	Lower Byte Data Strobe.
UDM0~UDM4	Upper Byte Input data mask.
LDM0~LDM4	Lower Byte data mask.
ODT	On Die Termination Enable.
VCC	Supply voltage.

Symbol	Description
GND	Ground.
VREF	Reference voltage.
NC	No connect.

5. DC OPERATING CONDITIONS

5.1. ABSOLUTE MAXIMUM DC RATINGS

Table-3 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Unit
VCC	Voltage on VCC pin relative to GND	-1.0 ~ 2.3	V
Vin, Vout	Voltage on any pin relative to GND	- 0.5 ~ 2.3	V
T_{OPR}	Operating Temperature Range	-40 ~ +105	℃
T_{STG}	Storage Temperature Range	-55 ~ +150	℃
I_I	Input Leakage Current	-5 to 5	uA
I_{OZ}	Output Leakage Current	-5 to 5	uA
I_{VREF}	VREF Leakage Current	-2 to 2	uA

5.2. Recommended DC Operating Conditions (SSTL_1.8)

Table-4 Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	1.7	1.8	1.9	V
V_{REF}	Input Reference Voltage	$0.49\times V_{CC}$	$0.50\times V_{CC}$	$0.51\times V_{CC}$	V
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V

6. TYPICAL APPLICATION

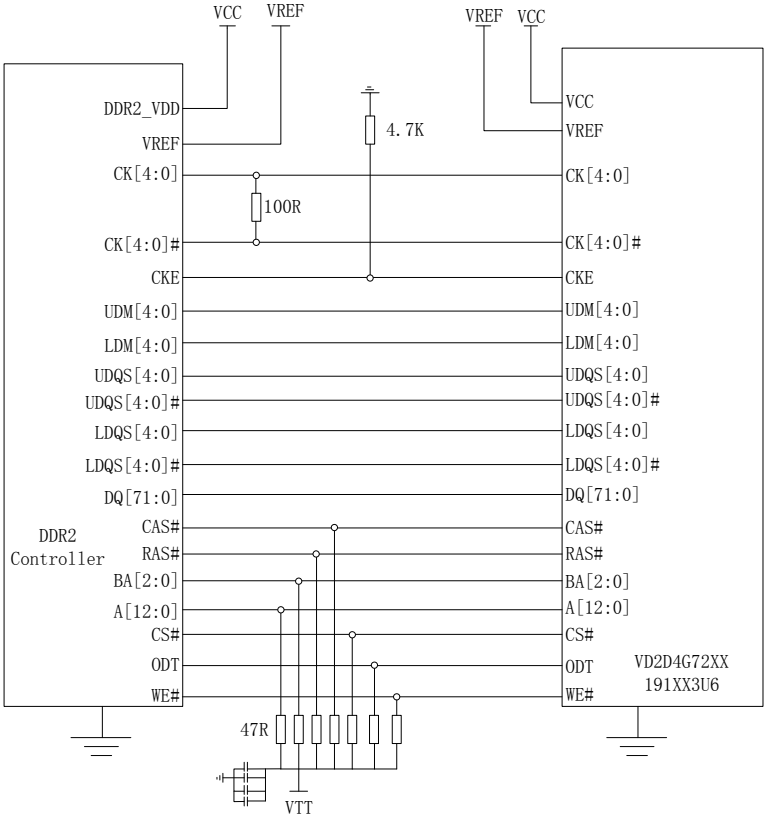

Figure-3 Typical application diagram

Table-5 VD2D4G72XB191XX3U6's Signal group

NO.	DQ	DQS	DM	CK	Address/Control
1	DQ[7:0]	LDQS0、LDQS0#	LDM0	CK0、CK0#	A[12:0]、BA[2:0]、CS#、CAS#、RAS#、WE#、CKE、ODT
2	DQ[15:8]	UDQS0、UDQS0#	UDM0		
3	DQ[23:16]	LDQS1、LDQS1#	LDM1	CK1、CK1#	
4	DQ[31:24]	UDQS1、UDQS1#	UDM1		
5	DQ[39:32]	LDQS2、LDQS2#	LDM2	CK2、CK2#	
6	DQ[47:40]	UDQS2、UDQS2#	UDM2		
7	DQ[55:48]	LDQS3、LDQS3#	LDM3	CK3、CK3#	
8	DQ[63:56]	UDQS3、UDQS3#	UDM3		
9	DQ[71:64]	LDQS4、LDQS4#	LDM4	CK4、CK4#	
10	-	UDQS4、UDQS4#	UDM4		

Note: 1. The A13 pin is reserved for future use,as an NC pin inside the memory module.
2. The chip corresponding to CK4 only has the lower 8 bits(DQ[71:64]),and the upper 8 bits are not taken out.

7. ORDERING INFORMATION

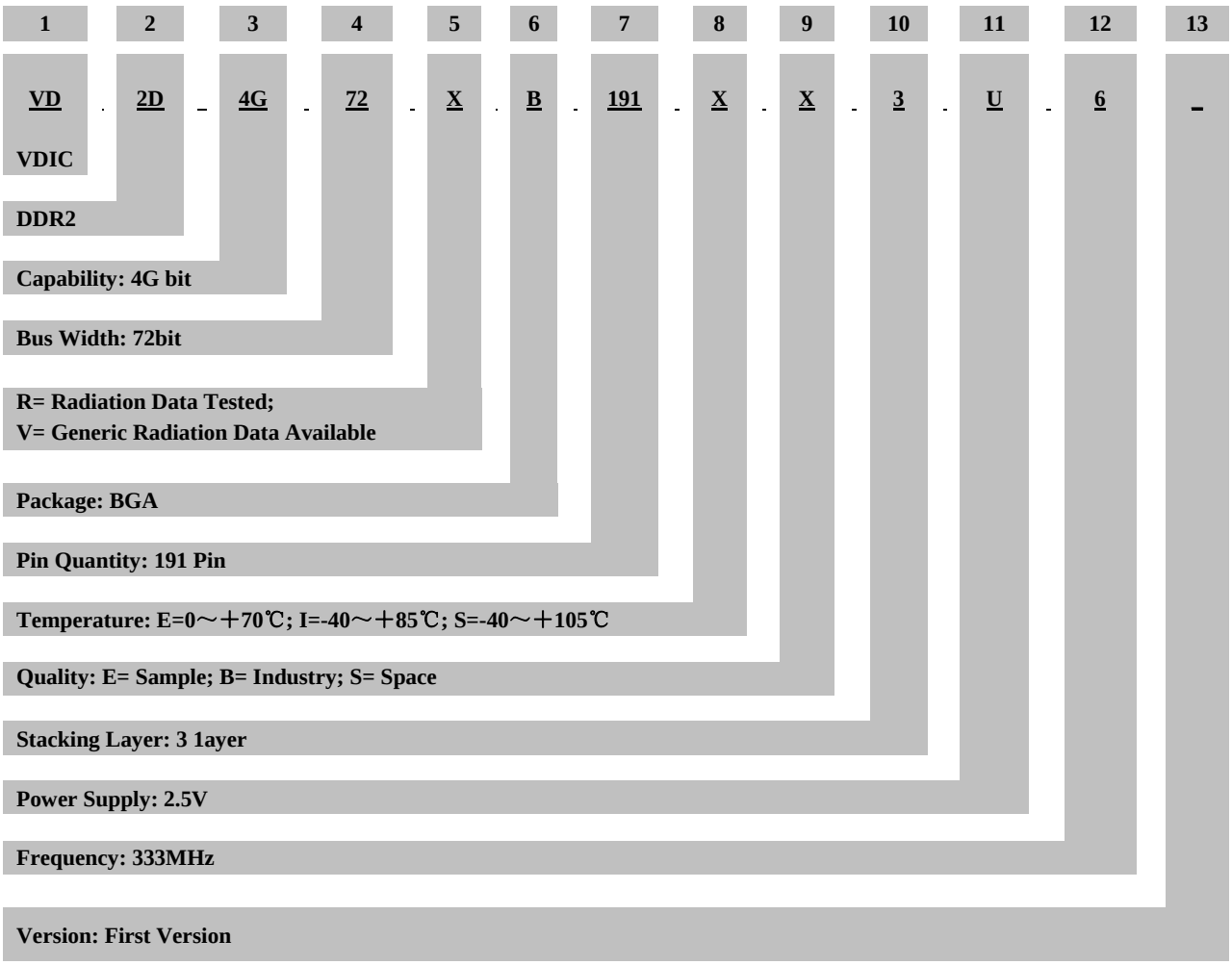

Table 6 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VD2D4G72VB191EE3U6	4G	72	-	-	-	BGA191	0 ~ +70
VD2D4G72VB191IB3U6	4G	72	-	-	-	BGA191	-40 ~ +85
VD2D4G72RB191SS3U6	4G	72	>100	>62.5	>2	BGA191	-40 ~ +105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

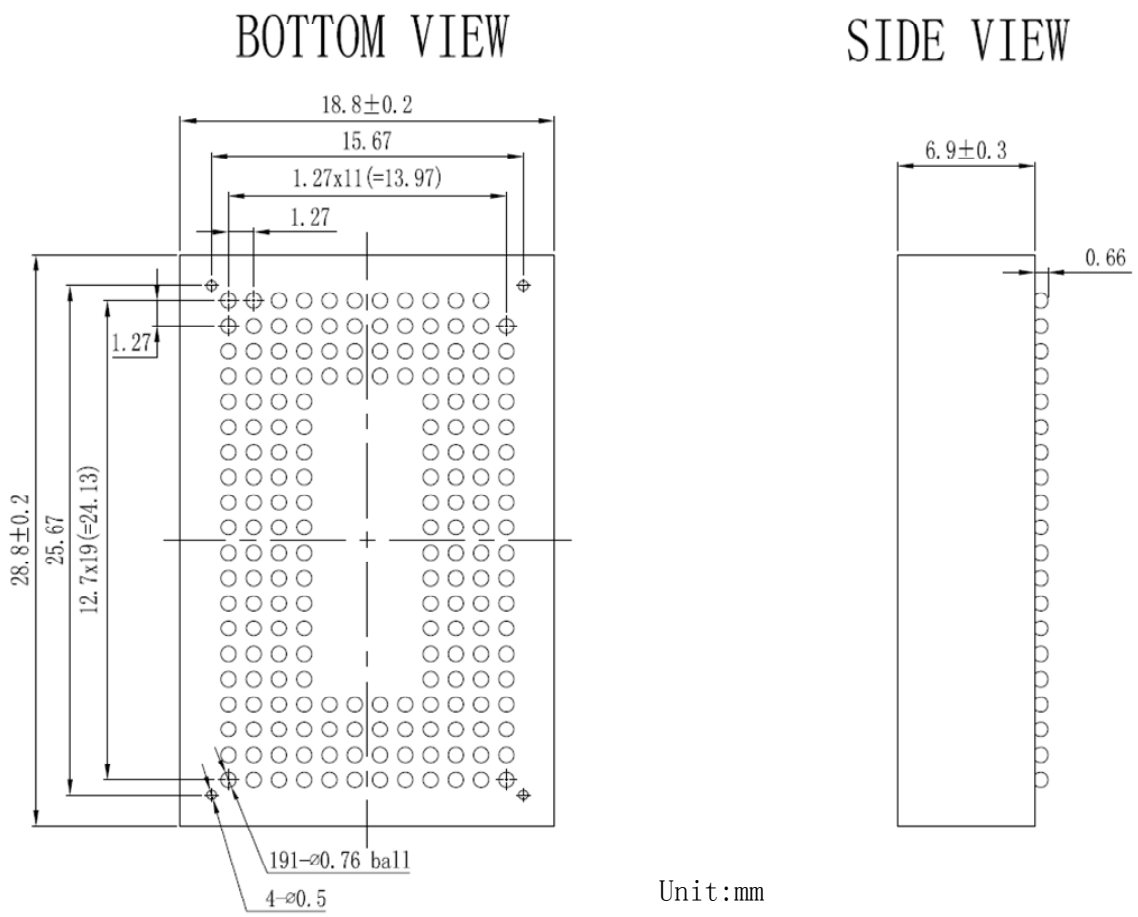

Figure-4 Package Dimensions

Table 7 Dimensions information

	Min	Max
A	7.26	7.86
A2	6.60	7.20
D	28.60	29.00
D1	24.13	
E	18.6	19.0
E1	13.97	
b	0.76	
e	1.27	
NOTE: 1.Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 8 Revision history

Revision	Date	Description of Change
A0	Nov. 5,2015	First Created.
A1	Mar. 15,2018	Add or reduce the chapters.
A2	Sept. 27,2018	Correct pin descriptions.
A3	Jan. 30,2019	Modified ordering information.
A4	Apr. 19,2019	Modified typical application.
A5	Apr. 26,2019	Change product name.
B0	Oct. 18,2019	1. Modify the description and some content. 2. Add Signal group.
B1	Mar 23,2020	Update TID and SEE