

VDIC QSPI NOR FLASH MEMORY

VDSF512M04XS18XX2V133 USER MANUAL

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VDIC-QSPI NOR Flash Memory

HIGH-SPEED 3.3V 512Mbit

1. DESCRIPTION

The VDSF512M04XS18XX2V133 is a 512Mbit high-density simultaneous Read/Write FLASH Memory module organized as 4× 128Mbit.

Using high-performance and high-reliability technology chips, stacking with the well-known ORBITA Proprietary technology, this FLASH memory module provides a cost-effective solution for low power and high-capacity non-volatile memory data storage needs.

Each device of the module is a 128Mbit QSPI FLASH Memory, organized 128 Mbit that can be accessed by activating the associated control signals(#CE、 #HOLD and #WP),and electrically erasable, read/write non-volatile flash memory. Any Page can be programmed typically in 0.2ms. The device features 3.3V voltage read and write operation, with frequency up to 133MHz. This device is designed to allow either single Sector / block or full Chip erase operation, where each Sector can be individually protected against program erase operations or temporarily unprotected to erase or program. The device can sustain a minimum of 1 million program erase cycles on each Sector. The VDSF512M04XS18XX2V133module is packaged in a SOP-18 package and is available for commercial, industrial and military temperature range.

2. FEATURES

Industry Standard Serial Interface

- VDSF512M04XS18XX2V133:512Mbit/64Mbyte
- 256 bytes per Programmable Page
- Supports standard SPI, Fast, Dual, Dual I/O, Quad I/O, SPI DTR, Dual I/O DTR, Quad I/O DTR, and QPI
- Double Transfer Rate (DTR) option
- Supports Serial Flash Discoverable Parameters (SFDP)(2)

High Performance Serial Flash (SPI)

- 133Mhz Fast Read at V_{cc}=2.7V to 3.6V
- 104Mhz Fast Read at V_{cc}=2.3V to 3.6V
- 532MHz equivalent at QPI operation
- 50MHz Normal Read
- DTR (Dual Transfer Rate) up to 66MHz
- Selectable dummy cycles
- Configurable drive strength
- Supports SPI Modes 0 and 3
- More than 100,000 erase/program cycles
- More than 20-year data retention

Flexible & Efficient Memory Architecture

- Chip Erase with Uniform Sector/Block Erase (4/32/64 Kbyte)
- Program 1 to 256 bytes per page
- Program/Erase Suspend & Resume

Efficient Read and Program modes

- Low Instruction Overhead Operations
- Continuous Read 8/16/32/64-Byte Burst Wrap
- Selectable burst length
- QPI for reduced instruction overhead

Low Power with Wide Temp. Ranges

- Single 2.3V to 3.6V Voltage Supply
- 5 mA Active Read Current
- 10 μ A Standby Current
- 5 μ A Deep Power Down

Advanced Security Protection

- Software and Hardware Write Protection
- Power Supply lock protect
- 128 bit Unique ID for each device (Call Factory)
- 18-lead SOP package

3. BLOCK DIAGRAM

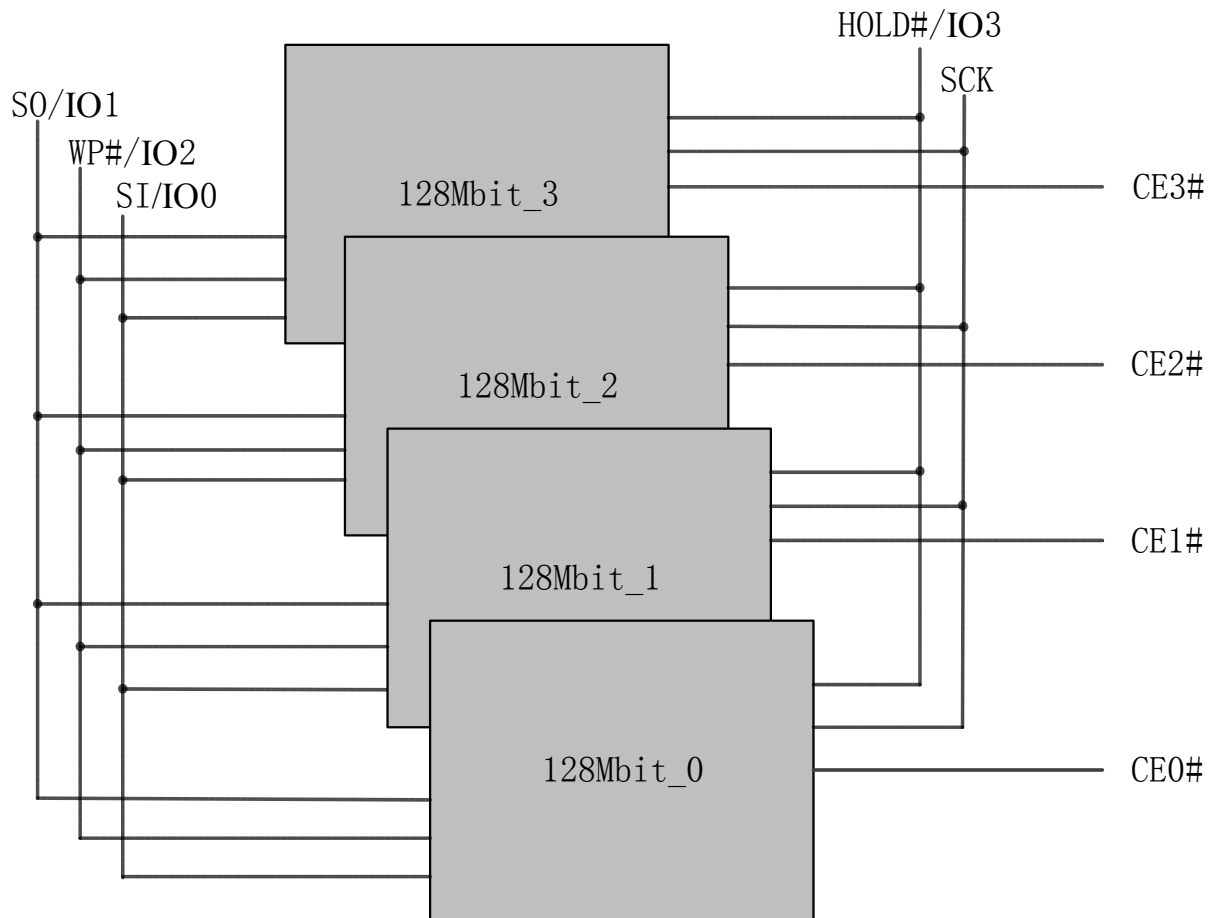


Figure 1 Block diagram

4. PIN DESCRIPTIONS– SOP-18

Pin Id	Pin #		Pin Id
CE1#	1	18	V _{cc}
RFU	2	17	CE3#
NC	3	16	RFU
GND	4	15	RFU
RFU	5	14	CE2#
CE0#	6	13	V _{cc}
SO/IO1	7	12	HOLD#/IO3
WP#/IO2	8	11	SCK
GND	9	10	SI/IO0

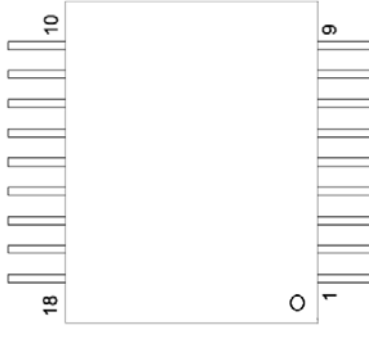


Figure 2 Pin configuration

Table 1 Pin description

Pin Name	Function
CE0#	Chip Enable 0
CE1#	Chip Enable 1
CE2#	Chip Enable 2
CE3#	Chip Enable 3
SI (IO0), SO (IO1)	Serial Data Input, Serial Output, and IOs (SI, SO, IO0, and IO1):
WP# (IO2)	Write Protect/Serial Data IO (IO2):
RFU	Reserved for Future Use
HOLD# or RESET# (IO3)	HOLD# or RESET#/Serial Data IO (IO3):
SCK	Serial Data Clock:
V _{cc}	Supply Voltage
GND	Ground
NC	Not Connected to anything

5. ELECTRICAL SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{cc} supply relative to V _{ss}	V _{cc}	-0.5 ~ +6.0	V
Input Voltage with Respect to GND on All Pins	V _T	-0.5 to V _{cc} + 0.5	V

Characteristics	Symbol	Maximum ratings	Unit
All Output Voltage with Respect to Ground	-	-0.5 to $V_{CC} + 0.5$	V
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_{OPR}	-40 ~ +105	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C

5.2 RECOMMENDED OPERATING RANGES

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.3	3.0	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{CC}$	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.5	—	$0.3 \times V_{CC}$	V

5.3 DC Characteristics Tables

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	$V_{CC} = 2.3V$, $V_{IL} = 0V$, $I_{OL} = 100 \mu A$	—	0.2	V
Output voltage high level	V_{OH}	$V_{CC} = 2.3V$, $V_{IH} = 0.9 \times V_{CC}$, $I_{OH} = -100 \mu A$	$V_{CC} - 0.2$	—	V

6. TYPICAL APPLICATION

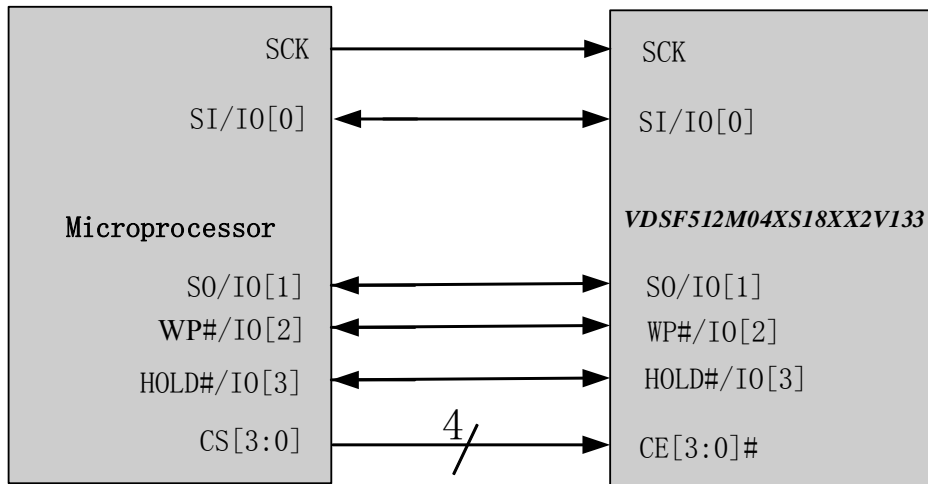


Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12
<u>VD</u>	<u>SF</u>	<u>512M</u>	<u>04</u>	<u>X</u>	<u>S</u>	<u>18</u>	<u>X</u>	<u>X</u>	<u>2</u>	<u>V</u>	<u>133</u>
VDIC											
QSPI NOR FLASH											
Capability: 512M bit											
Bus Width: 04bit											
R= Radiation Data Tested; V= Generic Radiation Data Available											
Package: SOP											
Pin Quantity: 18 Pin											
Temperature: E=0~+70℃; I=-40~+85℃; S=-40~+105℃											
Quality: E= Sample; B= Industry; S= Space											
Stacking Layer: 2layer											
Power Supply : 3.3V											
Frequency: 133MHz											

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSF512M04VS18EE2V133	512M	1/4	--	--	--	SOP18	0~+70
VDSF512M04VS18IB2V133	512M	1/4	-	-	-	SOP18	-40~+85
VDSF512M04VS18SS2V133	512M	1/4	TBD	TBD	TBD	SOP18	-40~+105

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8. PACKAGE DIMENSIONS

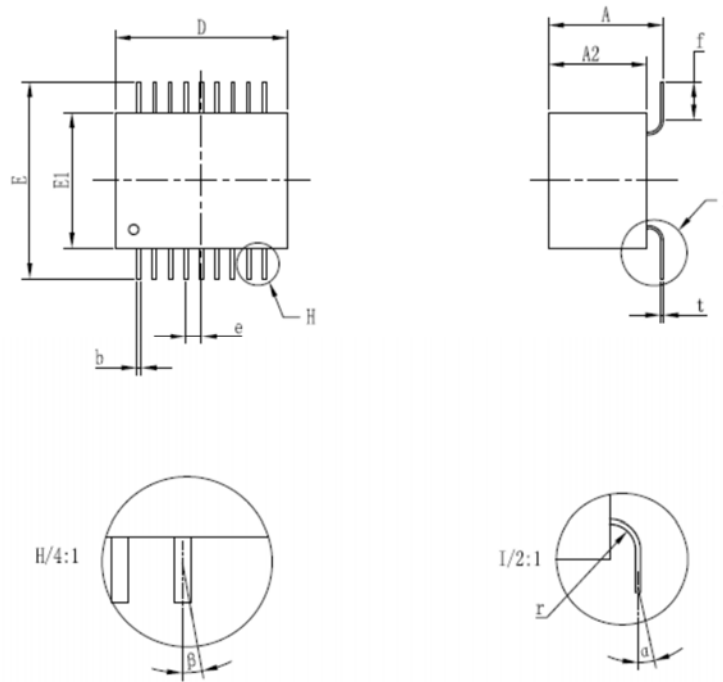


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	5.80	6.50
A2	4.60	5.20
D	13.80	14.20
E	15.70	16.10
E1	10.80	11.20
f	3.1	
b	0.35	
e	1.27	
t	0.2	
r	1.00	
α	$\leq 3^\circ$	
β	$\leq 3^\circ$	
NOTE: 1. Unit: mm 2. $A1 = A - A2$		

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	May 15,2020	First Created