VDIC
NOR FLASH MEMORY

VDRF2G08XS60XX4V90
USER MANUAL

Version :A0

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Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park, NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai, *Guangdong,* China 519080
Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

VDIC-NOR FLASH MEMORY

HIGH-SPEED 3.3V 256M × 8bit

1. DESCRIPTION

The VDRF2G08XS60XX4V90 is a 3.3V single power 2Gbit flash memory organized as 268.435.456 bytes.

It is organized in 4 banks with separate chip enable (#CE) controls. It requires only a single 3.3 Volt power supply for both read and write functions. In addition to V_{CC} input, a high-voltage accelerated program(#WP/A_{CC}) input provides shorter programming times through increased current.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The Enhanced control allows the host system to set the voltage levels that the device generates and tolerates on all input levels (address, chip control, and DQ input levels) to the same voltage level that is asserted on the V_{IO} pin . This allows the device to operate in a 1.8V or 3.3V system environment as required.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transistion. Persistent Sector protection provides in-system, command-enable protection of any combination of sectors using a single power supply at V_{CC}. Password sector Protection prevents unauthorized write and erase operations in any combination of sectors through a user-defined 64-bit password.

The VDRF2G08XS60XX4V90 module is packaged in a 60 pin sop package and is available in commercial, industrial and military temperature range.

2. FEATURES

- Single power supply operation

  3.3V read, erase, and program operations. All input levels (address, control, and DQ input levels) and output are determined by voltage on V_{IO} input V_{IO} range is 1.65 to V_{CC}.
- 100,000 erase cycles per sector typical.
- 20-year data retention typical.
- High performance.

  -110ns access time.

  -16byte page read buffer.

  -25ns page read times.

  -32-byte write buffer reduces overall programming time for multiple-word updates.
- Low power consumption.
- 60 pin SOP.
- Advanced Sector Protection.
- #WP/ACC input accelerates programming time.
- Hardware reset input
- Ready/#Busy output detects program or erase cycle completion.

3. BLOCK DIAGRAM

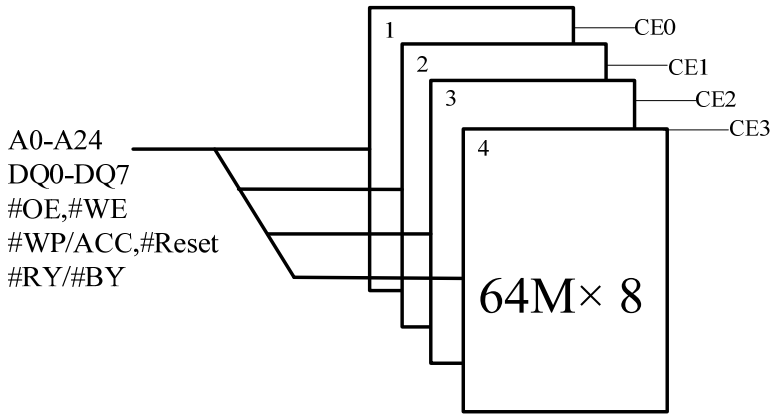

Figure 1 Block Diagram

4. PIN DESCRIPTIONS

Pin ID	Pin #		Pin ID
A23	1	60	A24
A22	2	59	NC
A15	3	58	A16
A14	4	57	NC
A13	5	56	VSS
A12	6	55	A-1
A11	7	54	DQ7
A10	8	53	NC
A9	9	52	DQ6
A8	10	51	NC
A19	11	50	DQ5
A20	12	49	NC
#WE	13	48	DQ4
#RESET	14	47	VCC
A21	15	46	NC
#WP/ACC	16	45	DQ3
RY/#BY	17	44	NC
A18	18	43	DQ2
A17	19	42	NC
A7	20	41	DQ1
A6	21	40	NC
A5	22	39	DQ0
A4	23	38	#OE
A3	24	37	VSS
A2	25	36	#CE0
A1	26	35	A0
NC	27	34	#CE1
NC	28	33	VIO
NC	29	32	#CE2
NC	30	31	#CE3

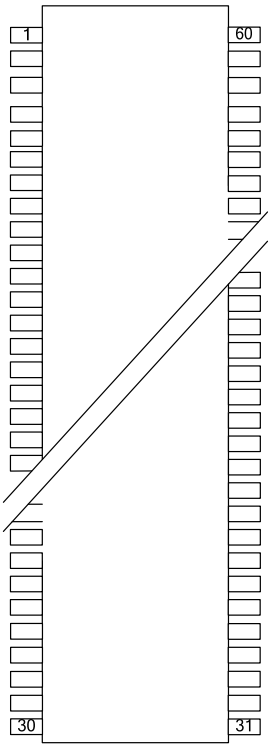

Figure 2 Pin configuration

Table 1 Pin description

Pin Name	Function
A0-A24	Address inputs
A-1	A-1 (LSB address input, in byte mode)
DQ0-DQ7	Data Inputs/Outputs
#CE [3:0]	Chip Enable
#OE	Output Enable
#WE	Write Enable
#WP/ACC	Write Protect / Acceleration Pin
#RESET	Hardware Reset Pin
VIO	Versatile IO input
RY/#BY	Ready/Busy Output
VCC	Device Power Supply
VSS	Ground
NC	Not Connected Internally

5. ELECTRICAL SPECIFICATIONS

5.1. Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to VSS	All Inputs and DQs except as noted below	-0.5 ~ V_{CC}+0.5	V
	V_{CC}	-0.5 ~ +4.0	
	V_{IO}	-0.5 ~ +4.0	
	A9 and ACC	-0.5 ~ +4.0	
Storage Temperature Range	T_{STG}	-65 ~ +150	℃
Operating Temperature Range	T_A	-55 ~ +125	℃
Power Dissipation	P_D	1.0	W
Reflow Temperature(Peak)	T_{SOL}	215	℃
Soldering Temperature Manual Reflow	T_M	250	℃
Thermal Resistance Junction to Case	$R_{TH(J-C)}$	20	℃/W

5.2. Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	0.7×V_{IO}	——	V_{IO} +0.3	V
Input low voltage	V_{IL}	-0.1	——	0.3×V_{IO}	V
V_{IO} Supply Voltage	V_{IO}	+1.65	——	V_{CC}	V

5.3. DC Characteristics

Table 4 DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.0V, I_{OL}=+100uA	——	0.40	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-100uA	2.3	——	V

6. TYPICAL APPLICATION

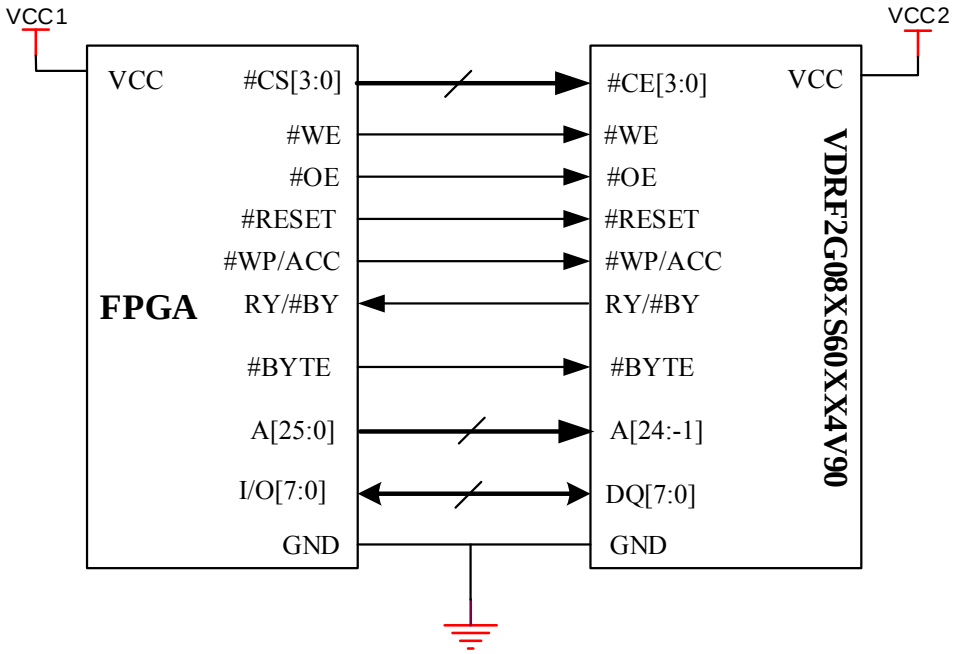

Figure 3 Typical application

7. ORDERING INFORMATION

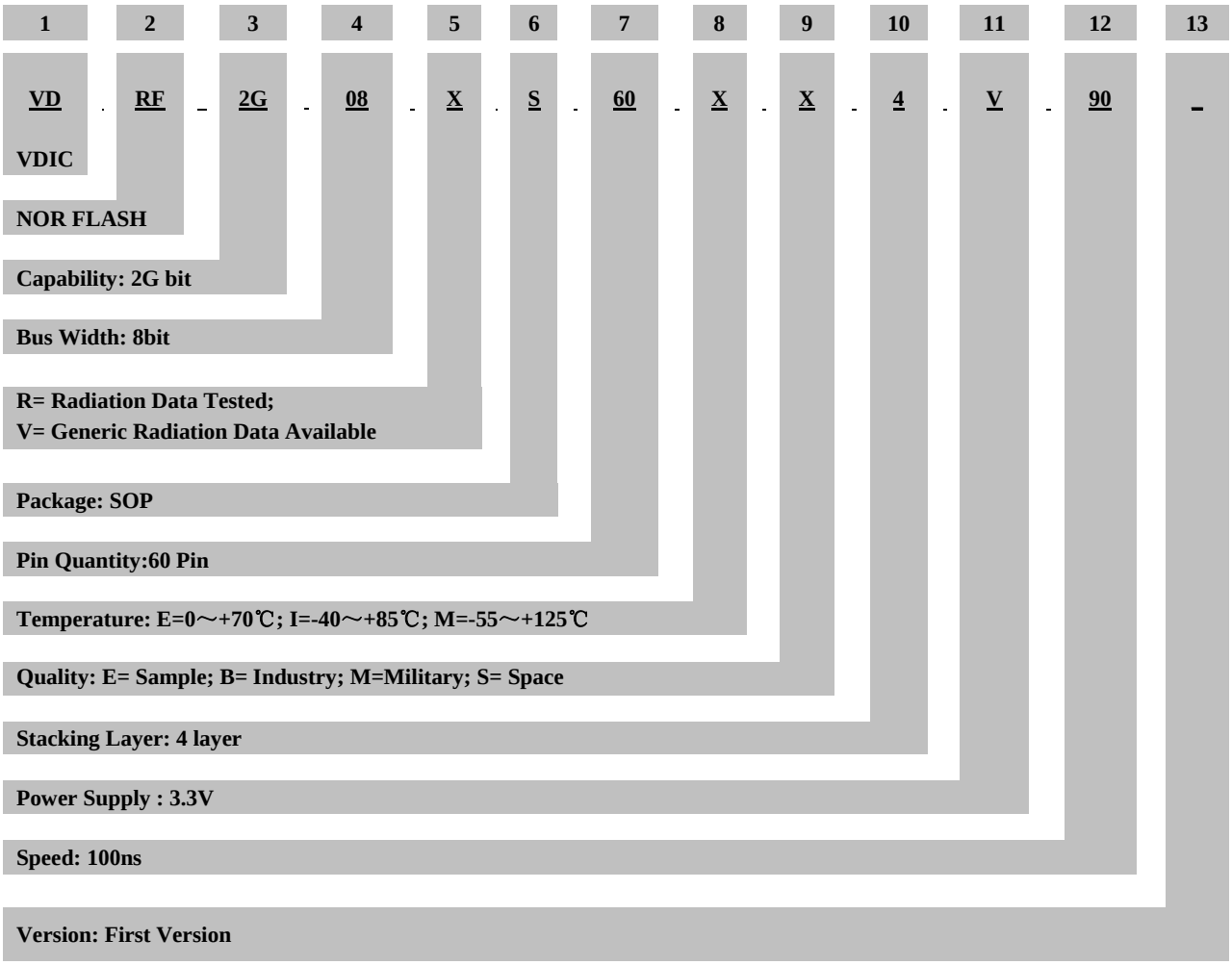

Table 5 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDRF2G08VS60EE4V90	2G	8	-	-	-	SOP60	0 ~ + 70
VDRF2G08VS60IB4V90			-	-	-		-40 ~ + 85
VDRF2G08VS60MM4V90			-	-	-		-55 ~ + 125
VDRF2G08RS60MS4V90			tbd	tbd	tbd		-55 ~ + 125

[1] TID: Total Dose Krads(Si)）
[2] SEL: LET Threshold（Mev.cm^2/mg）
[3] SEU: SEU Threshold （Mev.cm^2/mg）

8. PACKAGE DIMENSIONS

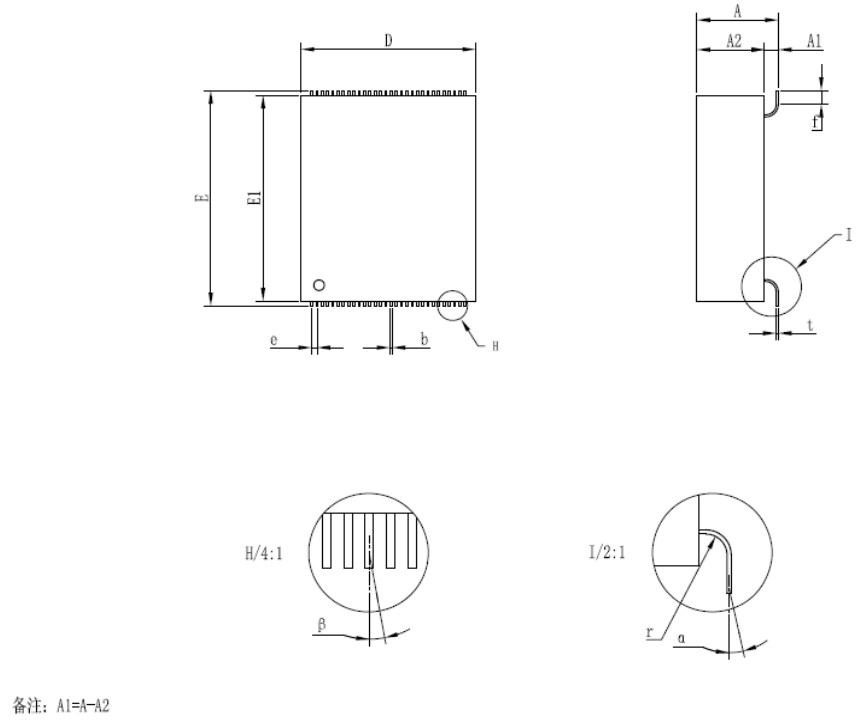

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	16.3	16.7
E	20.3	20.7
E1	19.4	19.8
f	1.30	
b	0.20	
e	0.50	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision History

Revision	Date	Description
A0	Nov 8, 2020	Initial Release