

**VDIC
MAGNETORESISTIVES
RANDOM ACCESS
MEMORY**

**VDMR20M40XS84XX5V35
USER MANUAL**

Version : B2

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VDIC-MRAM

HIGH-SPEED 3.3V 512K × 40bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1. DESCRIPTION

The VDMR20M40XS84XX5V35 is a $5 \times 4,194,304$ -bit high-speed access time, high-density Magnetoresistives Random Access Memory device. Manufactured with VDIC Very Dense SiP technology. It is organized as five independent dies of 512K x 8bit wide data interface.

The VDMR20M40XS84XX5V35 offers MRAM compatible 35ns read/write timing with unlimited endurance. Data is always non-volatile for greater than 20-years. Data is automatically protected on power loss by low-voltage inhibit circuitry to prevent writes with voltage out of specification. The VDMR20M40XS84XX5V35 is the ideal memory solution for applications that must permanently store and retrieve critical data and programs quickly.

The VDMR20M40XS84XX5V35 has five dies. Each die can be selected separately with dedicated #CEn. Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this MRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDMR20M40XS84XX5V35 is available in a 84-pin SOP package.

2. FEATURES

- Fast 35ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in a system for simpler, more efficient design
- Stack of five 4Mbit MRAM
- Organized as 5 dies of 512K x 8 bit memory
- Five independent Die Select
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- 84-lead SOP package

3. BLOCK DIAGRAM

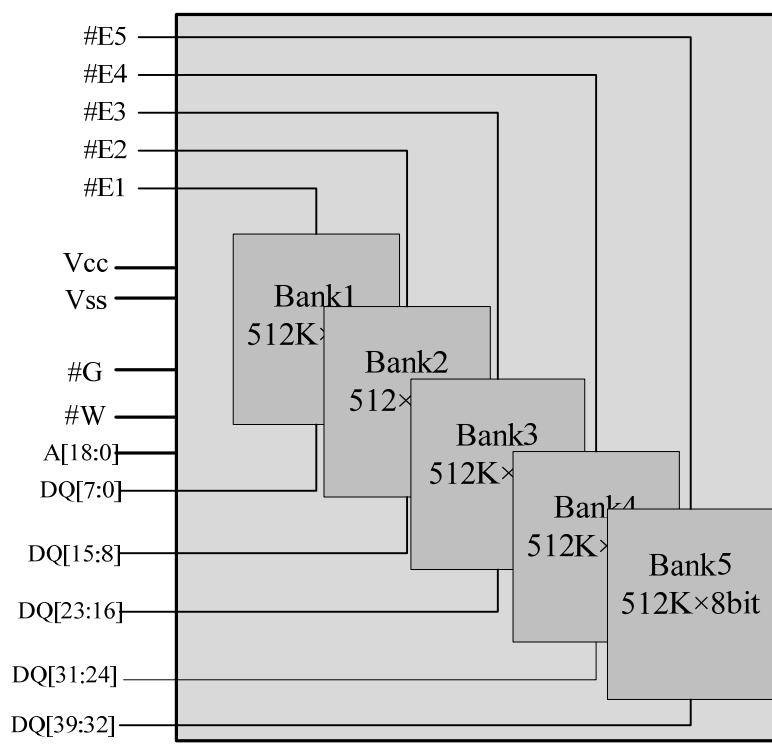


Figure 1 Block diagram

4. PIN DESCRIPTIONS

Pin Id	Pin #	Pin Id	
DQ33	1	84	NC
DQ32	2	83	NC
DQ25	3	82	#E5
DQ24	4	81	DQ38
#E4	5	80	DQ39
DQ17	6	79	DQ30
DQ16	7	78	DQ31
#E3	8	77	DQ22
DQ9	9	76	DQ23
DQ8	10	75	DQ14
DC1	11	74	DC8
#E2	12	73	DQ15
A0	13	72	DC7
A1	14	71	A18
A2	15	70	A17
A3	16	69	A16
A4	17	68	A15
#E1	18	67	#G
DQ0	19	66	DQ7
DQ1	20	65	DQ6
VDD	21	64	VSS
VSS	22	63	VDD
DQ2	23	62	DQ5
DQ3	24	61	DQ4
#W	25	60	DC6
A5	26	59	A14
A6	27	58	A13
A7	28	57	A12
A8	29	56	A11
A9	30	55	A10
DC2	31	54	DC5
DC3	32	53	DC4
DQ11	33	52	DQ12
DQ10	34	51	DQ13
DQ19	35	50	DQ20
DQ18	36	49	DQ21
DQ27	37	48	DQ28
DQ26	38	47	DQ29
DQ35	39	46	DQ36
DQ34	40	45	DQ37
NC	41	44	NC
NC	42	43	NC

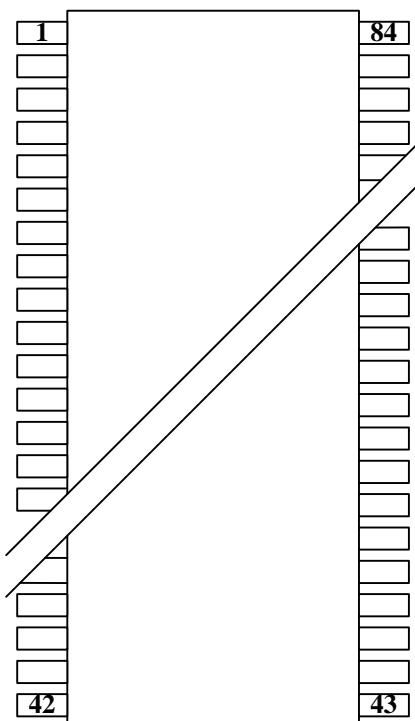


Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#E1	Die select	Disables or enables memory die1 operation
#E2	Die select	Disables or enables memory die2 operation
#E3	Die select	Disables or enables memory die3 operation
#E4	Die select	Disables or enables memory die4 operation
#E5	Die select	Disables or enables memory die5 operation
A0 ~ A18	Address	19-bit addresses
#W	Write enable	Enables write operation common to all memory dies
#G	Output enable	Enables data output common to all memory dies
DQ0~DQ39	Data input/output	Data inputs/outputs 40-bit wide bus
VDD/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	These pins are recommended to be left No Connection on the device.
DC1~DC8	Do not connect	These pins do not connect

5. ELECTRICAL SPECIFICATIONS

5.1. ABSOLUTE MAXIMUM RATINGS

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than the maximum rated voltages to these high-impedance (Hi-Z) circuits.

The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{DD} supply relative to Vss	V _{DD}	-0.5 ~ +4.0	V
Voltage on any pin relative to Vss	V _{IN}	-0.5 ~ V _{DD} +0.5	V
Power Dissipation	P _D	< 3.0	W
Operating Temperature Range	T _{OPR}	-55 ~ +95	°C
Storage Temperature Range	T _{STG}	-55 ~ +105	°C

5.2. RECOMMENDED DC OPERATING CONDITIONS

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{DD}	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.2	—	V _{DD} +0.3	V
Input low voltage	V _{IL}	-0.5	—	0.8	V
Write inhibit voltage	V _{WI}	2.5	2.7	3.0	V

5.3. DC ELECTRICAL CHARACTERISTICS

Table 4 DC electrical characteristics

PARAMETERS	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V _{OL}	I _{OL} = +4mA	—	0.4	V
Output voltage high level	V _{OH}	I _{OL} = -4mA	2.4	—	V

6. TYPICAL APPLICATION

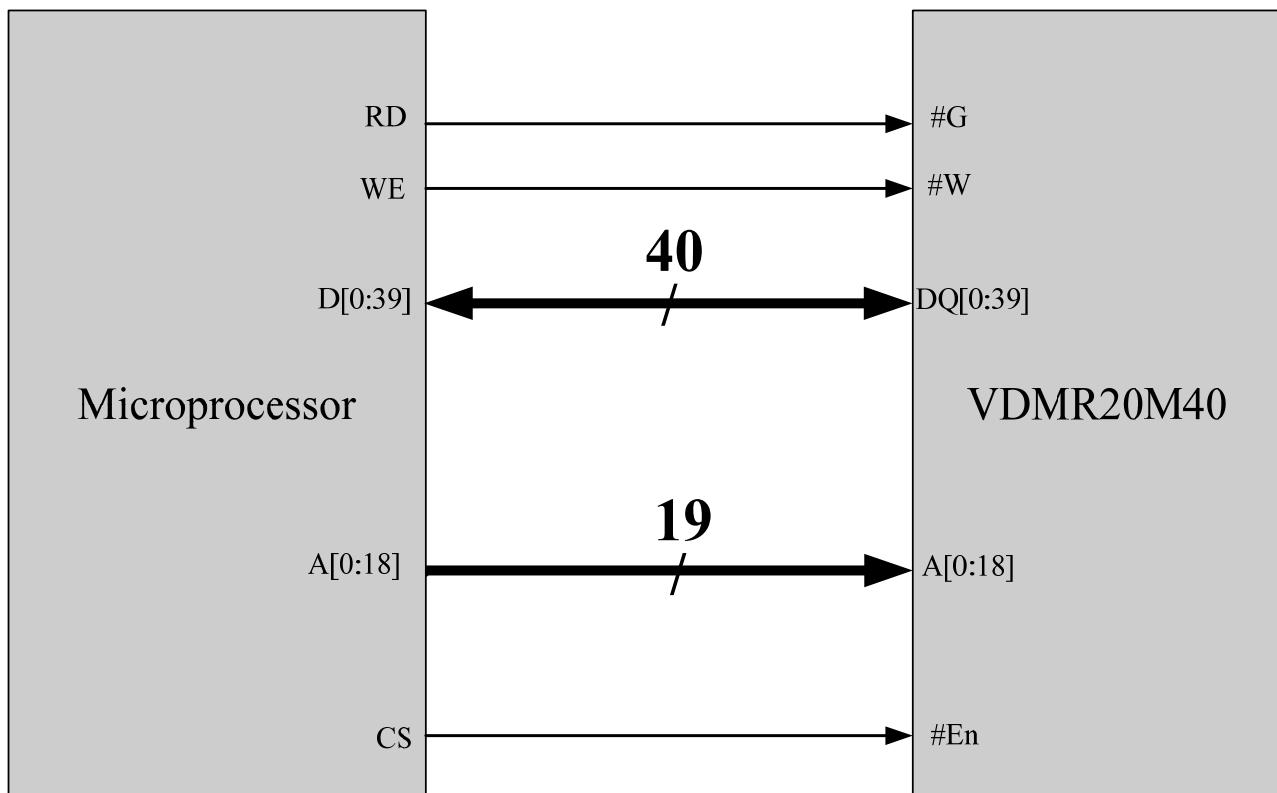


Figure 3 Typical application

7. ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>MR</u>	<u>20M</u>	<u>40</u>	<u>X</u>	<u>S</u>	<u>84</u>	<u>X</u>	<u>X</u>	<u>5</u>	<u>V</u>	<u>35</u>	-
VDIC												
MRAM												
Capability: 20M bit												
Bus Width: 40bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 84 Pin												
Temperature: E=0~+70°C; I=-40~+85°C; S=-55~+95°C												
Quality: E= Sample; B= Industry; S= Space												
Stacking Layer: 5 layer												
Power Supply : 3.3V												
Speed: 35ns												
Version: First Version												

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDMR20M40VS84EE5V35	20M	40	-	-	-	SOP84	0 ~ + 70
VDMR20M40VS84IB5V35	20M	40	-	-	-	SOP84	-40 ~ + 85
VDMR20M40RS84SS5V35	20M	40	TBD	TBD	TBD	SOP84	-55 ~ + 95

¹ TID: Total Dose (Krads(Si))

² SEL: LET Threshold (Mev.cm²/mg)

³ SEU:SEU Threshold (Mev.cm²/mg)

8. PACKAGE DIMENSIONS

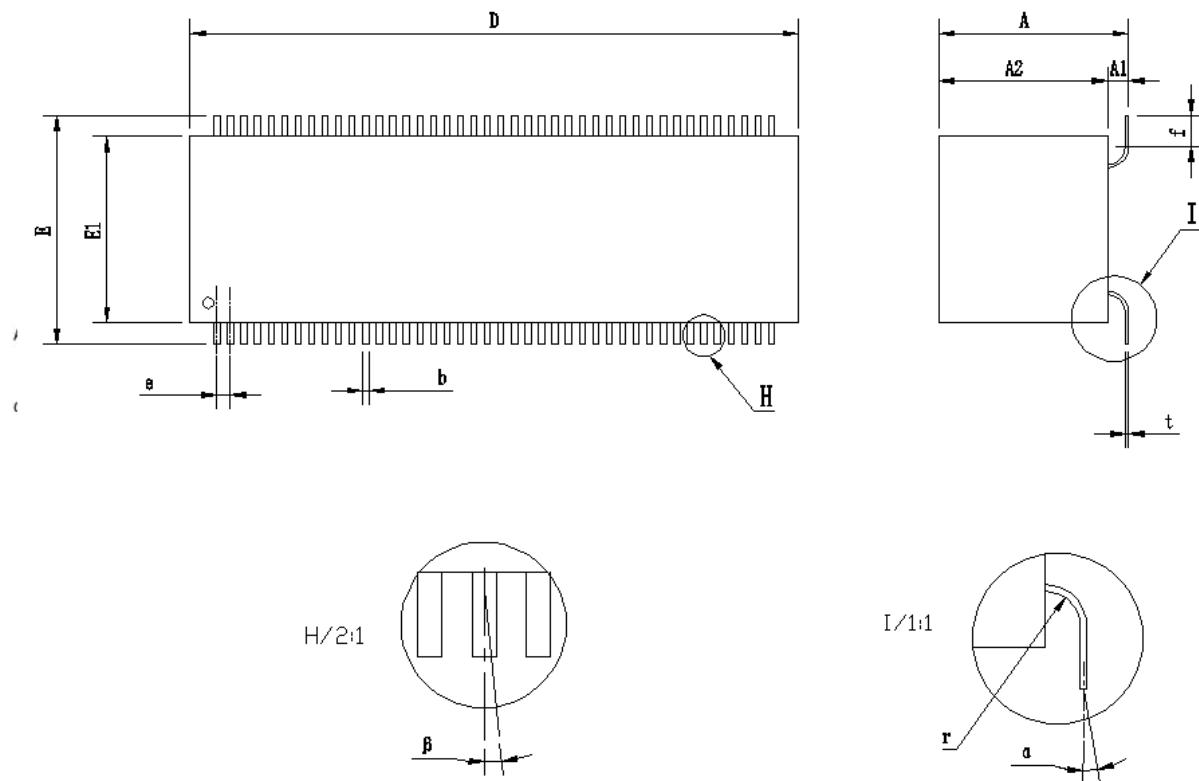


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	10.90	11.60
A2	9.70	10.30
D	35.80	36.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α		≤3°
β		≤3°

NOTE: 1. Unit: mm
2. A1=A - A2

9. REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Dec 26,2017	Add or reduce the chapters
B0	Mar 13,2018	Modified DC ELECTRICAL CHARACTERISTICS
B1	May 22, 2018	Modified Operating Temperature Range and Storage temperature.
B2	Mar 21,2020	Update TID and SEE