VDIC MAGNETORESISTIVES RANDOM ACCESS MEMORY

VDMR10M40XS96XX5V35 USER MANUAL

Version : A0

Document NO.: ORBITA/SIP- VDMR10M40XS96XX5V35-USM-01
Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.
Add: Orbita Tech Park, NO.1 Baisha Road，Tangjia Dong ` an，
Zhuhai, Guangdong, P.R. China 519080
Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

VDIC-MRAM

HIGH-SPEED 3.3V 256K × 40bit

MAGNETORESISTIVES RANDOM ACCESS MEMORY

1. Description

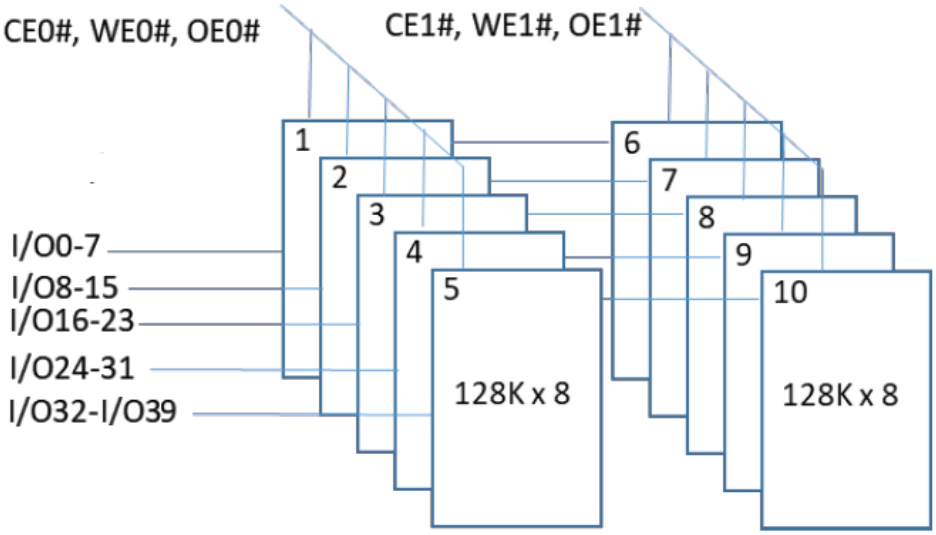
The Magnetoresistive Random Access Memory (MRAM) stores data using magnetic polarization rather than electric charge. The MRAM acts like a Flash (programmable) and like a SRAM (rapid data buffers). The VDMR10M40XS96XX5V35 is a high-speed highly integrated Static Random Access Memory containing 256K × 40bits, organized with two banks of 5Mbit. Each bank has a 40-bit interface and is selected with specific #En. It is particularly well suited for use in high reliability, high Performance and high density system applications. It is also targeted for systems demanding a very high reliability over Extreme temperature conditions and environments.

TheVDMR10M40XS96XX5V35 module is packaged in a 96 pin SOP.

2. Features

- Fast 35 ns Read/Write Cycle
- SRAM Compatible Timing, Uses Existing SRAM Controllers Without Redesign
- Unlimited Read & Write Endurance
- Data Always Non-volatile for >20-years at Temperature
- One Memory Replaces Flash, SRAM, EEPROM and BBSRAM in System for Simpler, More Efficient Design
- Replace battery-backed SRAM solutions with MRAM to eliminate battery assembly improving reliability
- 3.3 Volt Power Supply
- Automatic Data Protection on Power Loss
- Commercial, Industrial, Automotive Temperatures
- Package: SOP96

3. Block Diagram



(All other signals are common to the 10 memories)

Figure 1 Block Diagram

4. Pin Descriptions

Pin ID	Pin#		Pin#	Pin ID
VSS	1		49	VSS
A09	2		50	A16
A08	3		51	A15
A07	4		52	VCC
VCC	5		53	OE0#
A06	6		54	OE1#
A05	7		55	VSS
VSS	8		56	I/O39
I/O35	9		57	I/O31
I/O27	10		58	VCC
VCC	11		59	I/O23
I/O19	12		60	I/O15
I/O11	13		61	I/O07
I/O03	14		62	VSS
VSS	15		63	VSS
VCC	16		64	I/O06
I/O02	17		65	I/O14
I/O10	18		66	I/O22
I/O18	19		67	VCC
VSS	20		68	I/O30
I/O26	21		69	I/O38
I/O34	22		70	VSS
VCC	23		71	VCC
WE1#	24		72	CE0#
WE0#	25		73	CE1#
VSS	26		74	VSS
VCC	27		75	I/O33
I/O37	28		76	I/O25
I/O29	29		77	VCC
VSS	30		78	I/O17
I/O21	31		79	I/O09
I/O13	32		80	I/O01
I/O05	33		81	VSS
VCC	34		82	VCC
I/O04	35		83	I/O00
I/O12	36		84	I/O08
I/O20	37		85	I/O16
VSS	38		86	VSS
I/O28	39		87	I/O24
I/O36	40		88	I/O32
VCC	41		89	VCC
A14	42		90	A04
A13	43		91	A03
VSS	44		92	VSS
A12	45		93	A02
A11	46		94	A01
A10	47		95	A00
VCC	48		96	VCC

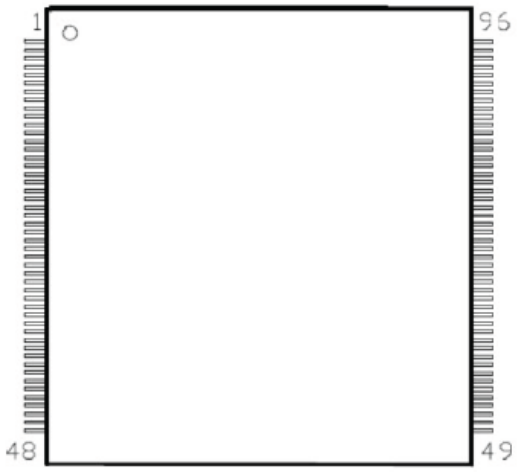


Figure 2 Pin Configuration

Table 1 Pin Description

Pin	Name	Function
#CE0	Die select	Disables or enables memory operation for die1,die2, die3 ,die4 and die5
#CE1	Die select	Disables or enables memory operation for die6,die7, die8 ,die9 and die10
A[16:0]	Address	17-bit addresses
#WE[1:0]	Write enable	Enables write operation common to all memory dies
#OE[1:0]	Output enable	Enables data output common to all memory dies
I/O[39:0]	Data input/output	Data inputs/outputs 40-bit wide bus
NC	No connection	These pins are recommended to be left No Connection on the device.
DC	Do not connect	These pins do not connect
VCC/VSS	Power supply/ground	Power and ground for the input/output buffers and core logic.

5. Electrical Specifications

5.1. Absolute Maximum Ratings

This device contains circuitry to protect the inputs against damage caused by high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage greater than maximum rated voltages to these high-impedance (Hi-Z) circuits. The device also contains protection against external magnetic fields. Precautions should be taken to avoid application of any magnetic field more intense than the maximum field intensity specified in the maximum ratings.

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Supply Voltage	V_{CC}	-0.5 ~ +4.0	V
Voltage on an pin	V_{IN}	-0.5 ~ V_{CC} +0.5	V
Operating Temperature Range	T_{OPR}	-55 ~ +95	℃
Storage Temperature Range	T_{STG}	-55 ~ +125	℃
Package Power Dissipation	P_D	4	W

5.2. Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

Parameter	Symbol	Min	T_{YP}	Max	Unit
Power Supply voltage	V_{CC}	3.0	3.3	3.6	V
Write inhibit voltage	V_{WI}	2.5	2.7	3.0	V
Input high voltage	V_{IH}	2.2	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.5	——	0.8	V

5.3. DC Characteristics

Table 4 DC Electrical Characteristics

Parameters	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	I_{OL}= +4mA	——	0.4	V
Output voltage high level	V_{OH}	I_{OL}= -4mA	2.4	——	V

6. Typical Application

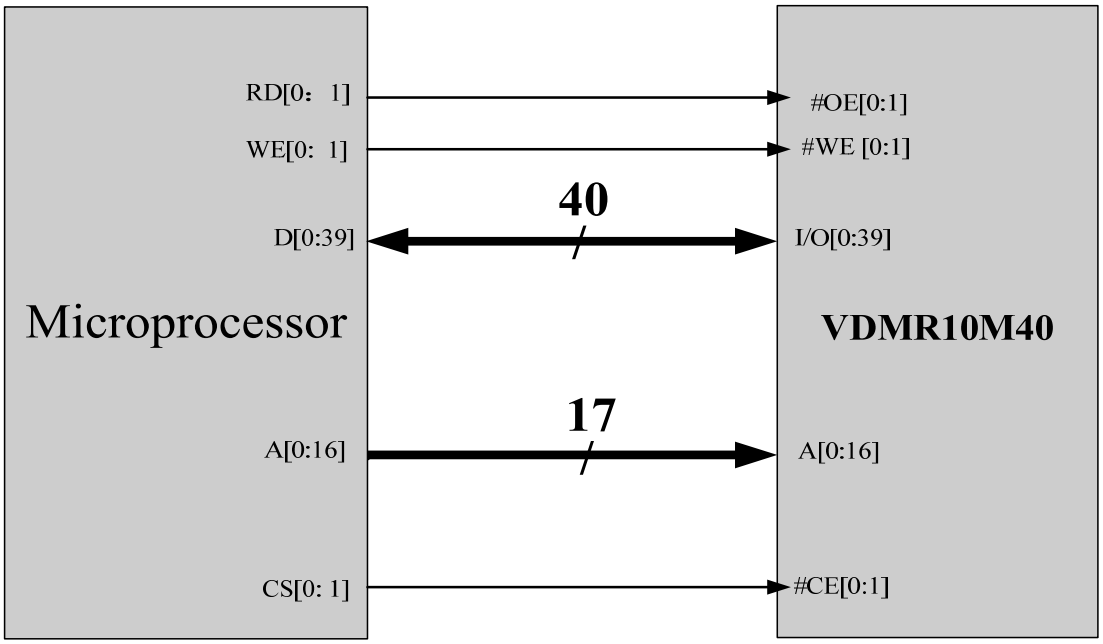


Figure 3 Typical Application

7. Ordering Information

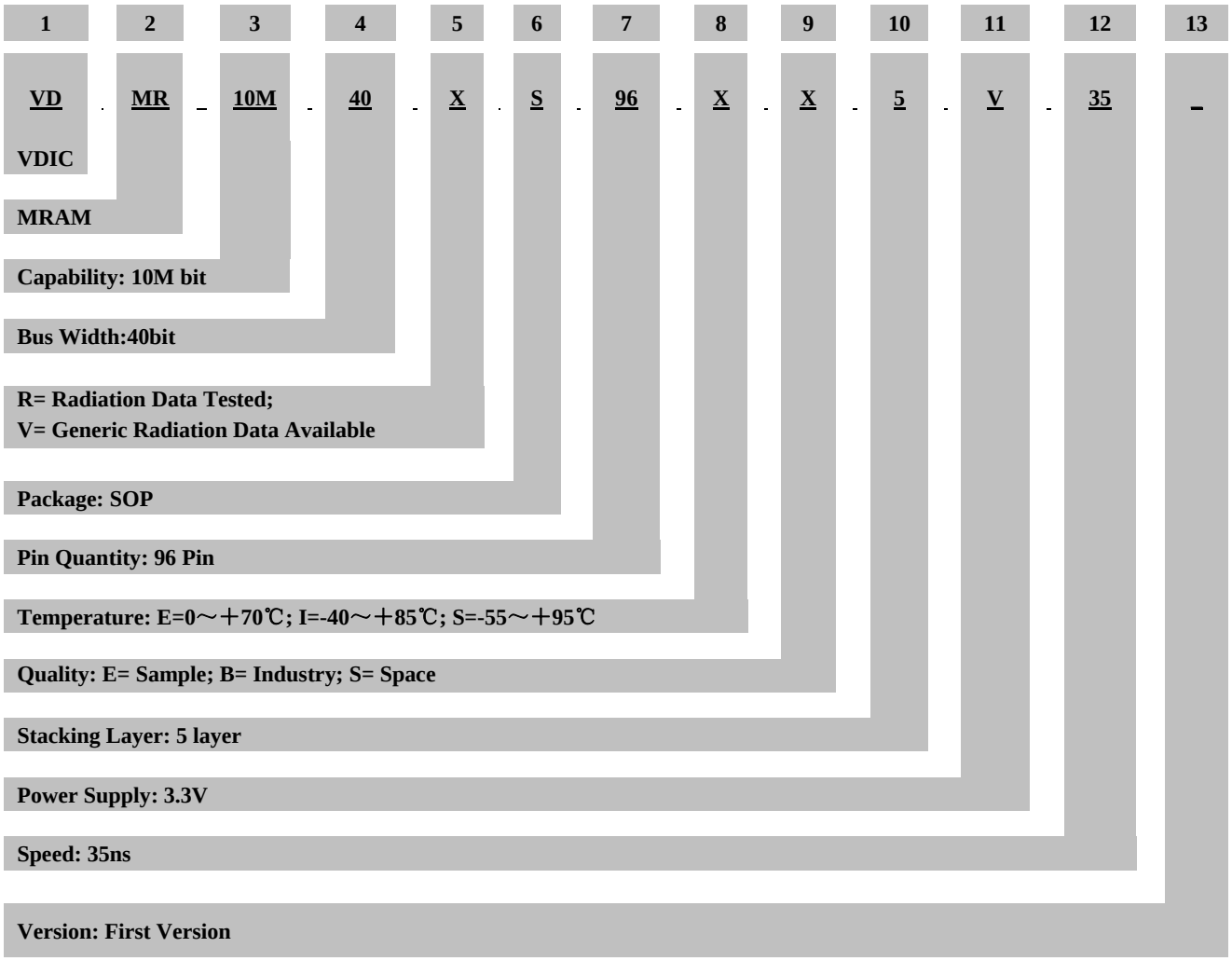


Table 5 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID (Krads(Si))	SEL (MeV.cm^2/mg)	SEU (MeV.cm^2/mg)		
VDMR10M40VS96EE8V35	10M	40	-	-	-	SOP96	0 ~ + 70
VDMR10M40VS96IB8V35		40	-	-	-	SOP96	-40 ~ + 85
VDMR10M40RS96SS8V35		40	> 50	> 80.3	< 14.2, > 9.3	SOP96	-55 ~ + 95

8. Package Dimensions

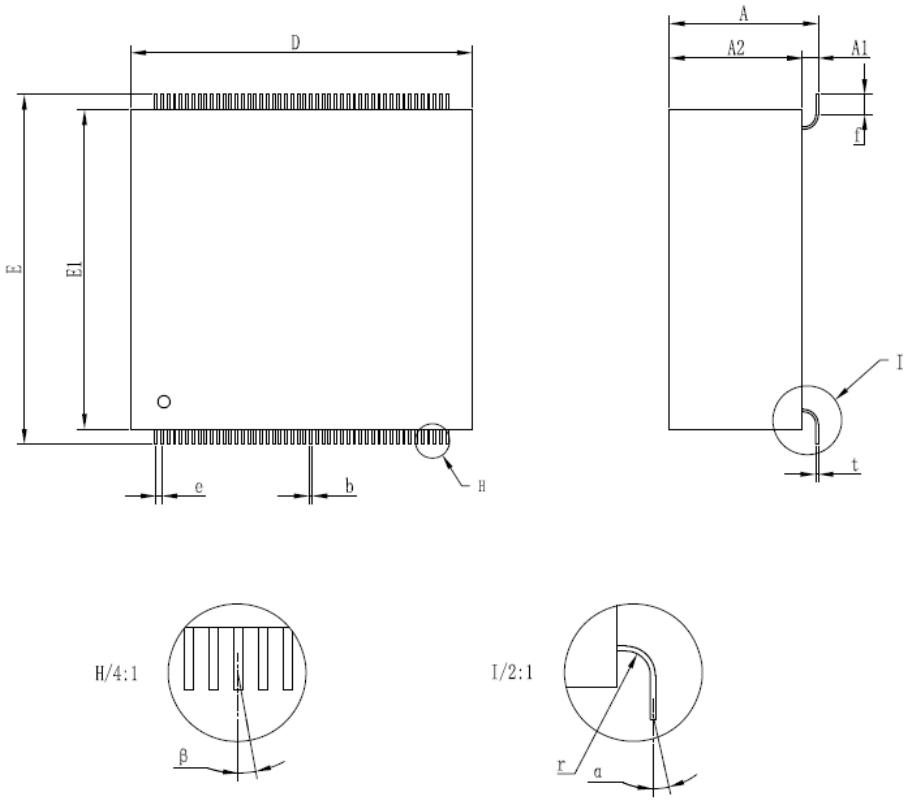


Figure 4 Package Dimensions

Table 6 Dimensions Information

	Min	Typical	Max
A	11.80	—	12.50
A2	10.60	—	11.20
D	27.80	—	28.20
E	28.50	—	28.90
E1	26.00	—	26.40
f	1.7		
b	0.2		
e	0.508		
r	1.00		
t	0.20		
α	≤3°		
β	≤3°		
NOTE: 1. Unit: mm 2. A1= A - A2			

9. Pads Designation

It is highly recommended to design pads as below.

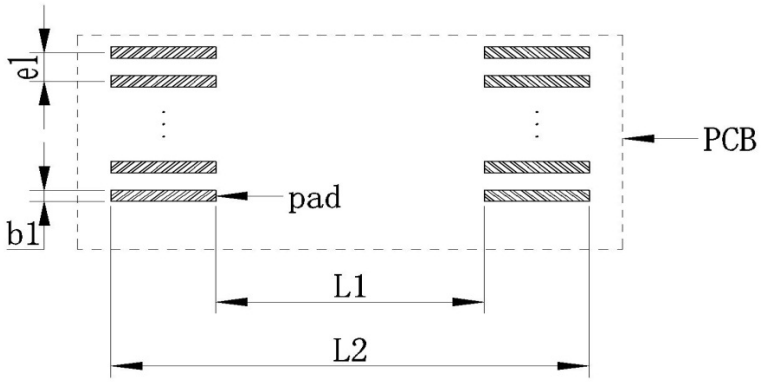


Figure 5 Pads Dimensions

NOTE:

e1: 0.508 mm;

b1: 0.3 mm;

L1: 22.1 mm;

L2: 29.9 mm.

10. Revision History

Table 7 Revision History

Revision	Date	Description of Change
A0	July 3,2021	Initial Release

s