VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD4G08XS58XX8V75 USER MANUAL

Version : A0

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VDIC-SDRAM

HIGH-SPEED 3.3V 512M×8bit

SYNCHRONOUS DYNAMIC SDRAM

1 Description

The VDSD4G08XS58XX8V75 is a high-speed highly integrated Synchronous Dynamic Random Access Memory containing 4,294,967,296 bits. It is organized with eight banks of 512 Mbit. Each bank has an 8-bit interface and is selected with specific #CS and CKE. It is particularity well suited for use in high reliability, high performance and high density system applications, such as solid state mass recorder, server or workstation.

The VDSD4G08XS58XX8V75 is packaged in a 58 pin SOP.

2 Features

- Single 3.3V ±0.3V power supply
- Clock frequency: 133MHz
- LVTTL interface
- Fully synchronous; all signalsreferenced to a positive clock edge
- Programmable burst length –(1,2,4, 8,full page)
- Programmable burst sequence: Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 58-pin SOP

3 Block Diagram

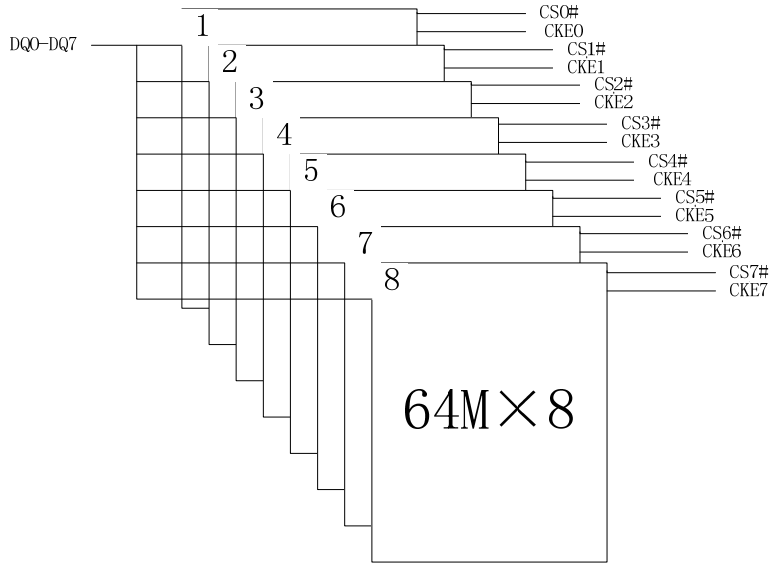

Figure 1 Block Diagram

4 Pin Descriptions

#CS7	1		58	**CKE7**
#CS6	2		57	**CKE6**
VDD	3		56	**VSS**
DQ0	4		55	**DQ7**
VDD	5		54	**VSS**
#CS5	6		53	**CKE5**
DQ1	7		52	**DQ6**
VSS	8		51	**VDD**
#CS4	9		50	**CKE4**
DQ2	10		49	**DQ5**
VDD	11		48	**VSS**
#CS3	12		47	**CKE3**
DQ3	13		46	**DQ4**
VSS	14		45	**VDD**
#CS2	15		44	**CKE2**
VDD	16		43	**VSS**
#CS1	17		42	**CKE1**
#WE	18		41	**DQM**
#CAS	19		40	**CLK**
#RAS	20		39	**CKE0**
#CS0	21		38	**A12**
BA0	22		37	**A11**
BA1	23		36	**A9**
A10	24		35	**A8**
A0	25		34	**A7**
A1	26		33	**A6**
A2	27		32	**A5**
A3	28		31	**A4**
VDD	29		30	**VSS**

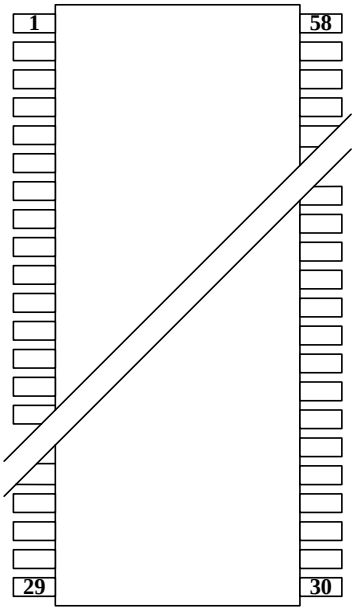

Figure 2 Pin Configuration

Table 1 Pin Description

Symbol	Type	Description
A0~A12	Input	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A0-A12) and READ or WRITE command (column address A0-A9,A11; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0~DQ7	I/O	Data Input/Output Ports.
#CS0~#CS7	Input	Chip select:#CSn enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CSn is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CSn is HIGH. #CSn provides for external bank selection on systems with multiple banks. #CSn is considered part of the command code.
BA[1:0]	Input	Bank address input(s): BA[1:0] defines to which bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
#RAS	Input	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Input	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Input	Write Enable Input. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
DQM	Input	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle.
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE0~CKE7	Input	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
V_{DD}	Supply	Power supply: +3.3V ±0.3V.
V_{SS}	Supply	Ground

5 Electrical Specifications

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}	-0.5 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ V_{DD} +0.5	V
Power Dissipation	P_D	2.0	W
Operating Temperature Range	T_{OPR}	-55 ~ +105	℃
Storage Temperature Range	T_{STG}	-65 ~ +125	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
	V_{IL}	-0.3	——	+0.8	V

5.3 DC Characteristics

Table 4 DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	V_{DD}=3.0V，I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	V_{DD}=3.0V，I_{OL}=2mA	——	0.4	V

6 Typical Application

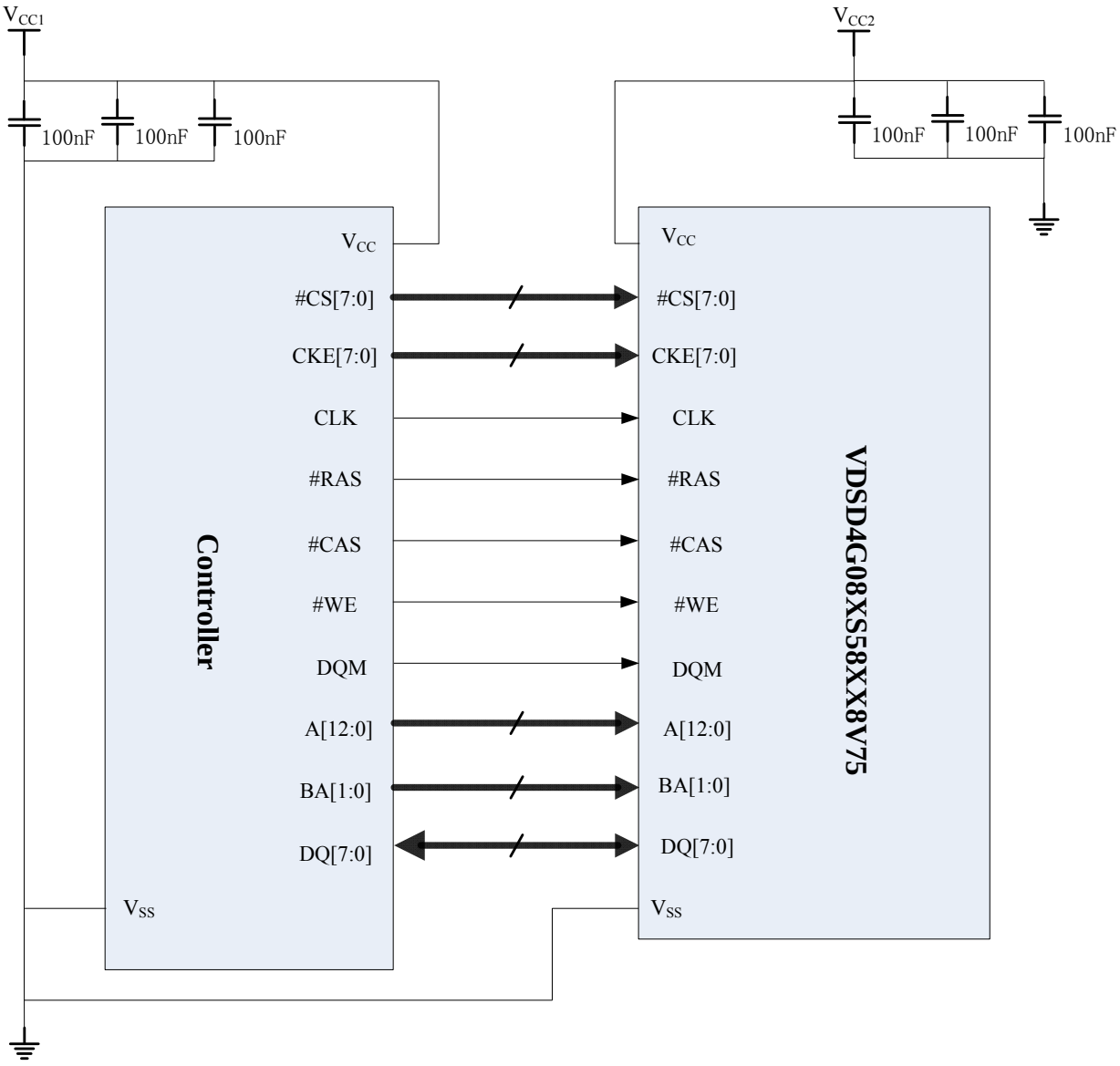

Figure 3 Typical Application

7 Ordering Information

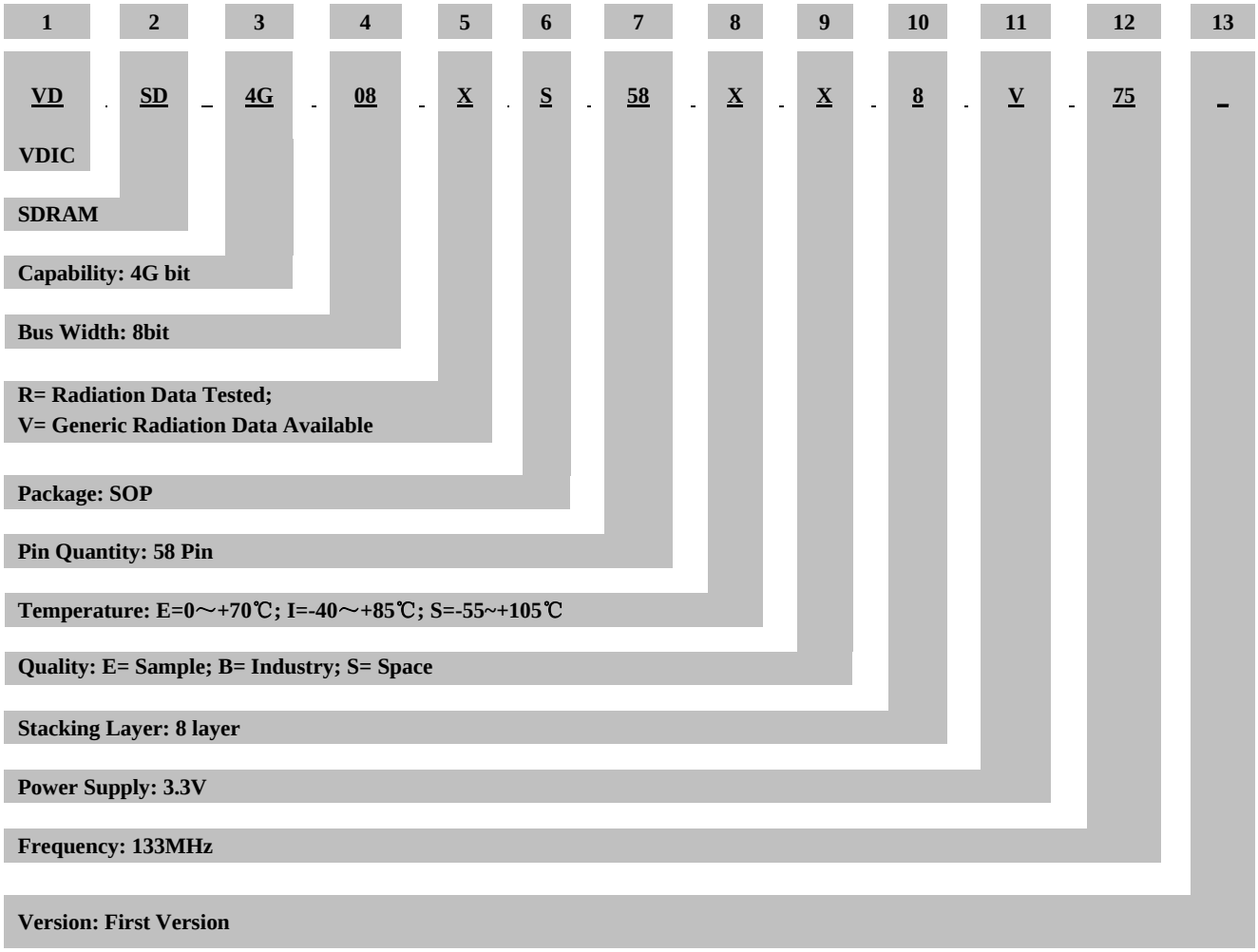

Table 5 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSD4G08VS58EE8V75	4G	8	-	-	-	SOP58	0 ~ + 70
VDSD4G08VS58IB8V75	4G	8	-	-	-	SOP58	-40 ~ + 85
VDSD4G08RS58SS8V75	4G	8	>50	> 80	2	SOP58	-55 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（MeV.cm^2/mg）
[3] SEU:SEU Threshold （MeV.cm^2/mg）

8 Package Dimensions

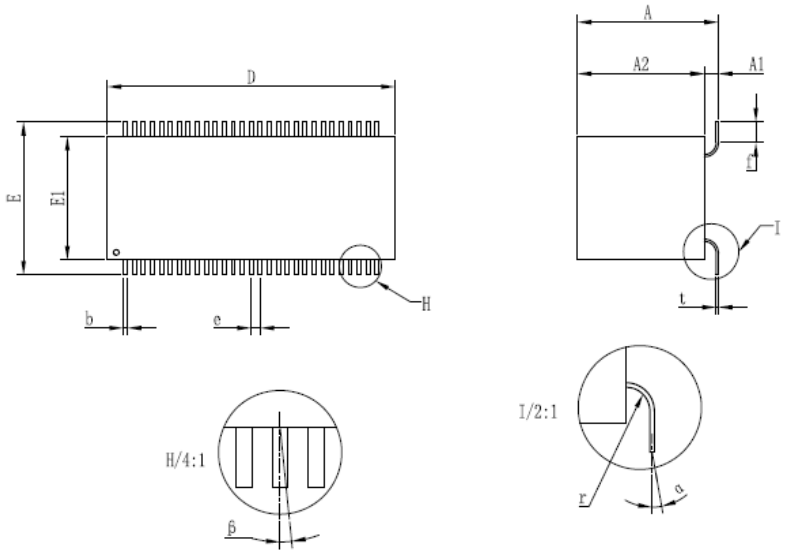

Figure 4 Package Dimensions

Table 6 Dimensions Information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	25.40	25.80
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.8	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1.U int: mm 2. A1= A - A2		

9 Pads Designation

It is highly recommended to design pads as below.

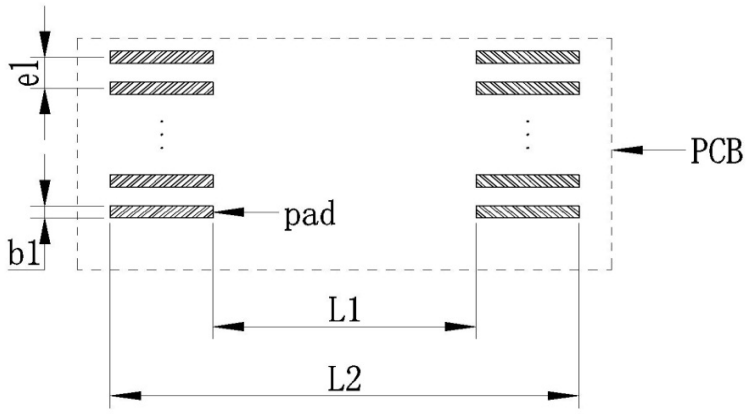

Figure 5 Pads Dimensions

NOTE:

e1: 0.8 mm;

b1: 0.5mm;

L1: 6.4mm;

L2: 14.8mm

10 Revision History

Table 7 Revision History

Revision	Date	Description
A0	Jun 1, 2021	Initial Release