

VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD4G08XS54XX8V75- II USER MANUAL

Version : B0

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Zhuhai Orbita Aerospace Science & Technology Co. , Ltd.

**Add: Orbita Tech Park, NO.1 Baisha Road , Tangjia Dong ` an ,
Zhuhai, Guangdong, China 519080**

Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

1	DESCRIPTION	1
2	FEATURES	1
3	BLOCK DIAGRAM	2
4	PIN DESCRIPTIONS	3
5	ELECTRICIAL SPECIFICATIONS.....	4
5.1	ABSOLUTE MAXIMUM RATINGS	4
5.2	RECOMMENDED DC OPERATING CONDITIONS.....	5
5.3	DC CHARACTERISTICS.....	5
6	TYPICAL APPLICATION	5
7	ORDERING INFORMATION	6
8	PACKAGE DIMENSIONS	6
9	REVISION HISTORY	8

VDIC-SDRAM

HIGH-SPEED 3.3V 512M×8Bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

The VDSD4G08XS54XX8V75- II is a 4,096M bits SDRAM, organized as 512M words×8bits. The device has 8 dies, each die includes 33,554,432 words×8bits×4bank, and a chip select. All inputs and outputs are referred to the rising edge of the clock. The device is useful for a variety of high bandwidth, high performance memory system applications. It is packaged in standard 54-pin TSOP.

2 FEATURES

- 3.3V power supply
- Clock frequency: 133MHz (max.)
- LVTTL interface
- Single pulsed #RAS
- 4 banks can operate simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length (BL): 1, 2, 4, 8, full page
- 2 variations of burst sequence
 - Sequential (BL=1, 2, 4, 8, full page)
 - Interleave (B =1, 2, 4, 8)
- Programmable #CAS latency (CL): 2, 3
- Refresh cycles: 8192 refresh cycles/64ms
- 2 variations of refresh
 - Auto refresh
 - Self refresh

3 BLOCK DIAGRAM

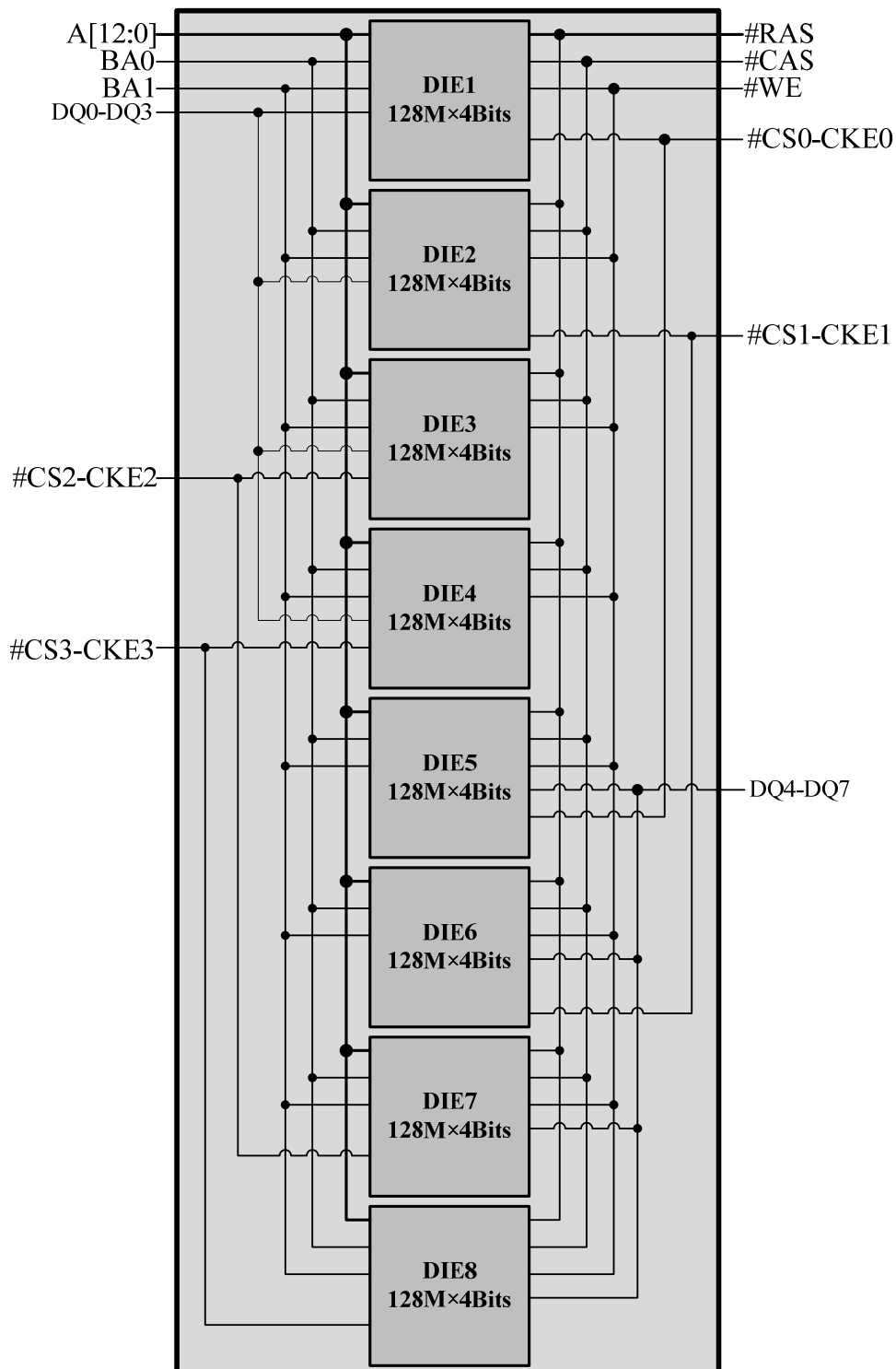


Figure 1: Signal link of Block Diagram

4 PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
VDD	1	54	VSS
NC	2	53	CKE3
VDDQ	3	52	VSSQ
DQ4	4	51	DQ7
DQ0	5	50	DQ3
VSSQ	6	49	VDDQ
#CS3	7	48	CKE2
#CS2	8	47	CKE1
VDDQ	9	46	VSSQ
DQ5	10	45	DQ6
DQ1	11	44	DQ2
VSSQ	12	43	VDDQ
#CS1	13	42	NC
VDD	14	41	VSS
NC	15	40	NC
#WE	16	39	DQM
#CAS	17	38	CLK
#RAS	18	37	CKE0
#CS0	19	36	A12
BA0	20	35	A11
BA1	21	34	A9
A10	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
VDD	27	28	VSS

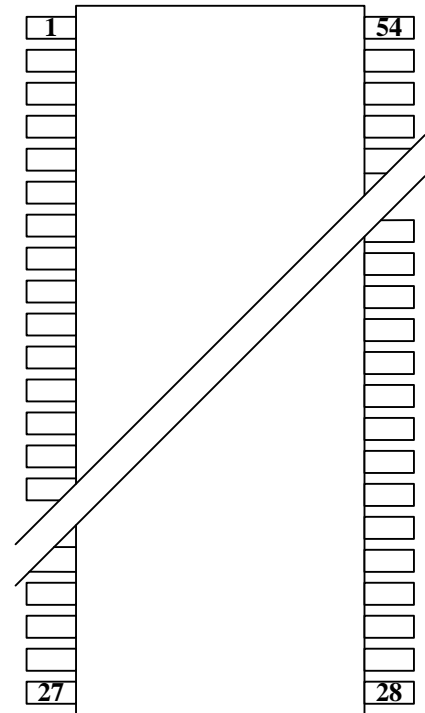


Figure 1 Pin configuration

Table 1 Pin Descriptions

Name	Function
A0~A12	Address Input. Row address (AX0 to AX12) is determined by A0 to A12 at the bank active command cycle CLK rising edge. Column address is determined by A0 to A9, A11 or A12 at the read or write command cycle CLK rising edge. And this column address becomes burst access start address.
DQ0-DQ7	Data Input/Output Ports. 8 bi-directional ports are used to read data from, or write data into the SDRAM.
#CS0 (Die1)	Die Enable Input. When #CSn is Low, the command input cycle becomes valid. When #CSn is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
#CS1 (Die2)	
#CS2 (Die3)	
#CS3 (Die4)	

Name	Function
BA0,BA1	BA0 and BA1 are bank select signal (BS).
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Write Enable Input.. Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
DQM	DQM controls input/output buffers. Read operation: If DQM is High, the output buffer becomes High-Z. If the DQM is Low, the output buffer becomes Low-Z. (The latency of DQM during reading is 2 clocks.) Write operation: If DQM is High, the previous data is held (the new data is not written). If DQM is Low, the data is written. (The latency of DQM during writing is 0 clock.)
CLK	CLK is the master clock input to this pin. The other input signals are referred at CLK rising edge.
CKE0~CKE3	Clock enable. This pin determines whether or not the next CLK is valid. If CKE is High, the next CLK rising edge is valid. If CKE is Low, the next CLK rising edge is invalid. This pin is used for power-down mode, clock suspend mode and self-refresh mode.
V _{DD}	Power supply, connect to 3.3V. V _{DD} are power supply pins for internal circuits.
V _{DDQ}	Power supply, connect to 3.3V. V _{DDQ} are power supply pins for the output circuits.
V _{SS}	Ground. V _{SS} are power supply pins for internal circuits
V _{SSQ}	Ground. V _{SSQ} are power supply pins for the output circuits.
NC	No connect

NOTE: A10 defines the precharge mode. When A10=High at the precharge command cycle, all banks are precharged. But when A10=Low at the precharge command cycle, only the bank that is selected by BA0 and BA1 (BS) is precharged. For details refer to the command operation section.

5 ELECTRICAL SPECIFICATIONS

- All voltages are referenced to V_{SS} (GND).
- After power up, execute power up sequence and initialization sequence before proper device operation is achieved (refer to the Power-up Sequence).

5.1 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V _{DD} supply relative to V _{SS}	V _{DD} / V _{DDQ}	-0.5 ~ +4.6	V
Voltage on any pin relative to V _{SS}	V _{IN}	-0.5 ~ V _{DD} +0.5(≤ 4.6 (max))	V
Power Dissipation	P _D	2.0	W
Operating Temperature Range	T _{OPR}	-55 ~ +105	°C
Storage Temperature Range	T _{STG}	-65 ~ +150	°C

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage/ DQ power	V _{DD} / V _{DDQ}	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.0	—	V _{DD} +0.3	V
Input low voltage	V _{IL}	-0.3	—	0.8	V

5.3 DC Characteristics

Table 4 DC Characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V _{OH}	V _{DD} =3.0V, I _{OH} =-2mA	2.4	—	V
Output Low Voltage Level	V _{OL}	V _{DD} =3.6V, I _{OL} =2mA	—	0.4	V

6 TYPICAL APPLICATION

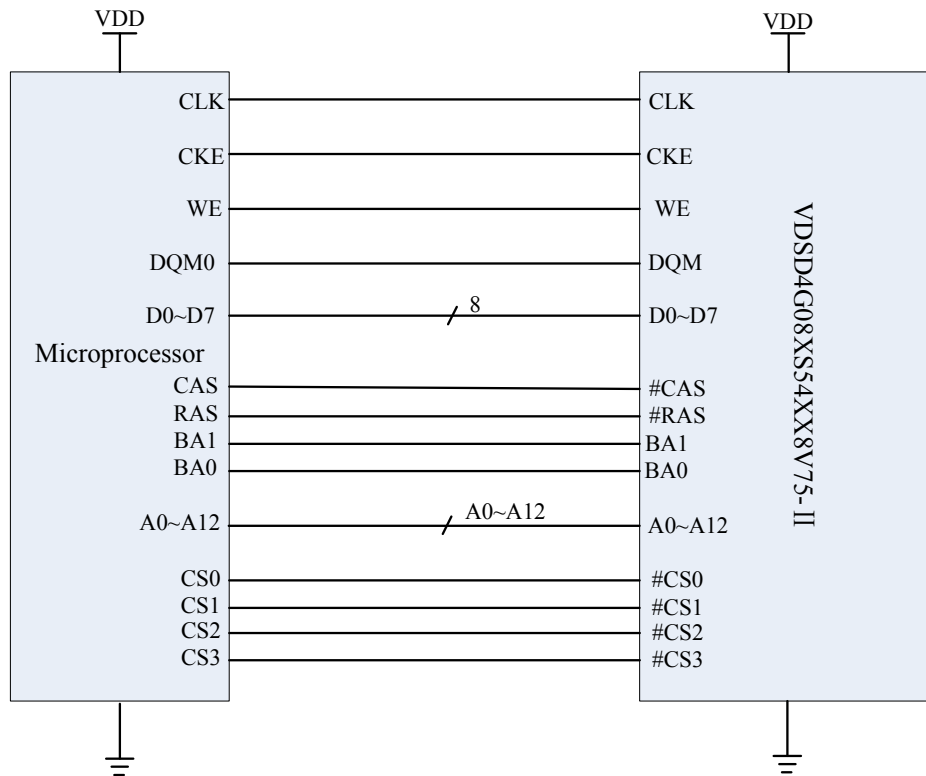


Figure 2 Typical application

7 ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
<u>VD</u>	<u>SD</u>	<u>4G</u>	<u>08</u>	<u>X</u>	<u>S</u>	<u>54</u>	<u>X</u>	<u>X</u>	<u>8</u>	<u>V</u>	<u>75</u>	<u>II</u>
VDIC												
SDRAM												
Capability: 4G bit												
Bus Width: 8bit												
R= Radiation Data Tested; V= Generic Radiation Data Available												
Package: SOP												
Pin Quantity: 54 Pin												
Temperature: E=0~+70°C; I=-40~+85°C; S=-55~+105°C												
Quality: E= Sample; B= Industry; S= Space												
Stacking Layer: 8layer												
Power Supply : 3.3V												
Frequency: 133MHz												
II=Second Version												

Table 5 Ordering Information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (°C)
			TID ¹	SEL ²	SEU ³		
VDSD4G08VS54EE8V75- II	4G	8	-	-	-	SOP54	0 ~ + 70
VDSD4G08VS54IB8V75- II	4G	8	-	-	-	SOP54	-40 ~ + 85
VDSD4G08RS54SS8V75- II	4G	8	>50	TBD	TBD	SOP54	-55 ~ + 105

¹ TID: Total Dose (Krad(Si))

² SEL: LET Threshold (Mev.cm2/mg)

³ SEU:SEU Threshold (Mev.cm2/mg)

8 PACKAGE DIMENSIONS

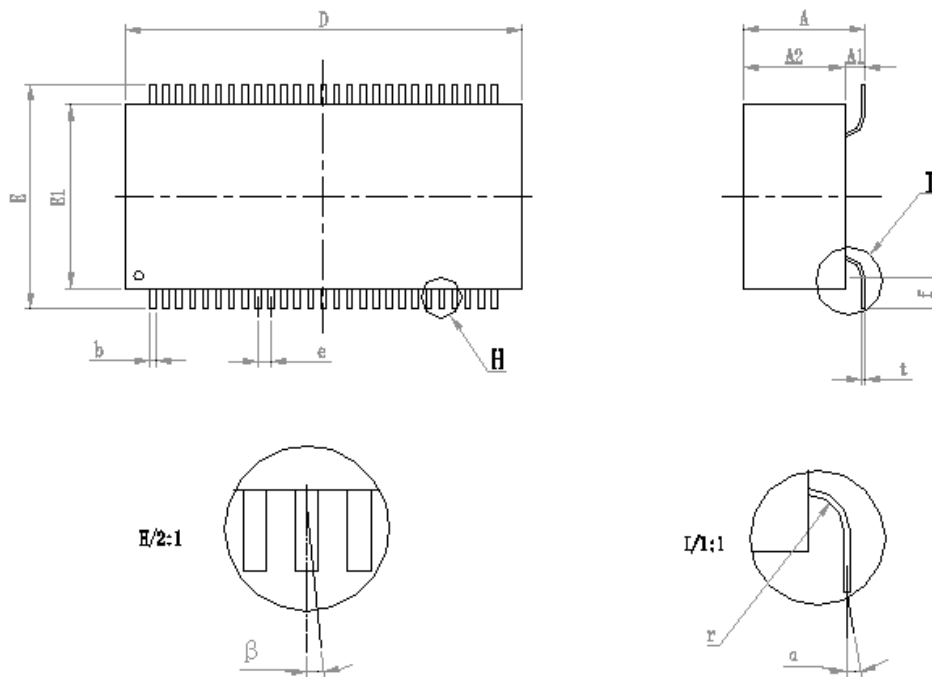


Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	7.40	7.90
A2	6.20	6.60
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
alpha	≤3°	
beta	≤3°	
NOTE: 1. Unit: mm 2. A1=A - A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the Truth Table
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co., Ltd
A5	Mar 3,2018	Modified ORDERING INFORMATION
B0	Mar 19,2020	Update format