VDIC SYNCHRONOUS DYNAMIC SDRAM

VDSD1G32XS70XX2V75 USER MANUAL

Version : B3

Contents

VDIC-SDRAM

HIGH-SPEED 3.3V 32M × 32bit

SYNCHRONOUS DYNAMIC SDRAM

1 DESCRIPTION

The VDSD1G32XS70XX2V75 is a 1,024M bits SDRAM, organized as 32M words×32bits. The device has two dies, every die includes a 8,388,608×16bits×4 bank, and two chip select individual signals. All inputs and outputs are referred to the rising edge of the clock input. This allows the device to be useful for a variety of high bandwidth, high performance memory system applications. It is packaged in 70-pin SOP.

2 FEATURES

- Single 3.3V ±0.3V power supply
- Clock frequency: 133MHz
- LVTTL interface
- Fully synchronous; all signals referenced to a positive clock edge
- Programmable burst length –(1,2,4,   8,full page)
- Programmable burst sequence: Sequential/Interleave
- Auto Refresh (CBR)
- Self Refresh
- Random column address every clock cycle
- Programmable #CAS latency (2,3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- It is packaged in 70-pin SOP

3 BLOCK DIAGRAM
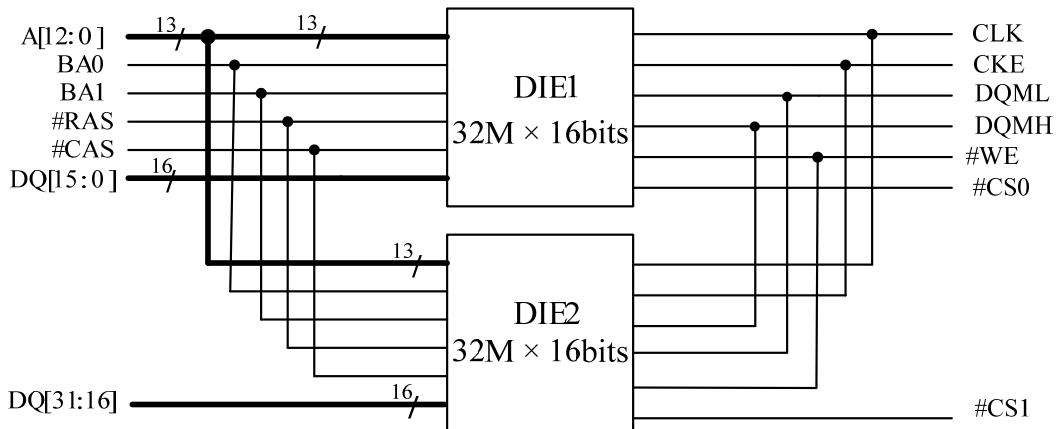
Figure 1: Signal link of Block Diagram

4 PIN DESCRIPTIONS

Pin Id	Pin #		Pin Id
VDD	1	70	VSS
DQ0	2	69	DQ31
DQ16	3	68	DQ15
VDDQ	4	67	VSSQ
DQ1	5	66	DQ30
DQ17	6	65	DQ14
DQ2	7	64	DQ29
DQ18	8	63	DQ13
VSSQ	9	62	VDDQ
DQ3	10	61	DQ28
DQ19	11	60	DQ12
DQ4	12	59	DQ27
DQ20	13	58	DQ11
VDDQ	14	57	VSSQ
DQ5	15	56	DQ26
DQ21	16	55	DQ10
DQ6	17	54	DQ25
DQ22	18	53	DQ9
VSSQ	19	52	VDDQ
DQ7	20	51	DQ24
DQ23	21	50	DQ8
VDD	22	49	VSS
LDQM	23	48	UDQM
#WE	24	47	CLK
#CAS	25	46	CKE
#RAS	26	45	A12
#CS0	27	44	A11
#CS1	28	43	A9
BA0	29	42	A8
BA1	30	41	A7
A10	31	40	A6
A0	32	39	A5
A1	33	38	A4
A2	34	37	A3
VDD	35	36	VSS
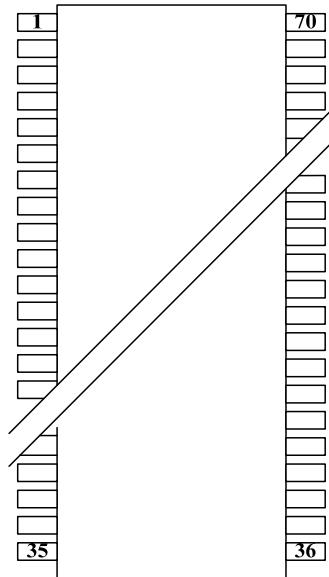
Figure 1 Pin configuration

Table 1 Pin description

Name	Function
A0~A12	Address inputs: A[12:0] are sampled during the ACTIVE command (row address A[12:0]) and READ or WRITE command (column address A[9:0]; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by A10 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0-DQ31	Data Input/Output Ports: 8 bi-directional ports are used to read data from or write data into the SDRAM.
#CS0 (Die1) #CS1 (Die2)	Chip select: #CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when #CS is registered HIGH, but READ/WRITE bursts already in progress will continue, and DQM operation will retain its DQ mask capability while #CS is HIGH. #CS provides for external bank selection on systems with multiple banks. #CS is considered part of the command code.
BA0,BA1	Bank address input(s): BA[1:0] defines to which bank the ACTIVE,READ,WRITE,or PRECHARGE command is being applied.
#RAS	Row address strobe: Latches row addresses on the positive going edge of the CLK with #RAS low. Enables row access & precharge.
#CAS	Column address strobe: Latches column addresses on the positive going edge of the CLK with #CAS low. Enables column access.
#WE	Write Enable Input: Enables write operation and row precharge. Latches data in starting from #CAS, #WE active.
LDQM,UDQM	Input/output mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses.Input data is masked when DQM is sampled HIGH during a WRITE cycle.The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. LDQM corresponds to DQ[7:0] and DQ[23:15],and UDQM corresponds to DQ[15:8] and DQ[31:24].LDQM and UDQM are considered same state when referenced as DQM.
CLK	Clock: CLK is driven by the system clock.All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Clock enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge power-down and SELF REFRESH operation (all banks idle), active power-down (row active in any bank), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
VDDQ	DQ power: DQ power to the die for improved noise imminity.
VSSQ	DQ ground: DQ ground to the die for improved noise imminity.
VDD	Power supply: 3.3V±0.3V.
VSS	Ground.
NC	No connection.

5 ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-0.5 ~ +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 ~ V_{DD} +0.5	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 ~ +105	℃
Storage Temperature Range	T_{STG}	-65 ~ +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{DD}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.8	V

5.3 DC Characteristics

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output High Voltage Level	V_{OH}	V_{DD}=3.0V , I_{OH}=-2mA	2.4	——	V
Output Low Voltage Level	V_{OL}	V_{DD}=3.6V , I_{OL}=2mA	——	0.4	V

6 TYPICAL APPLICATION
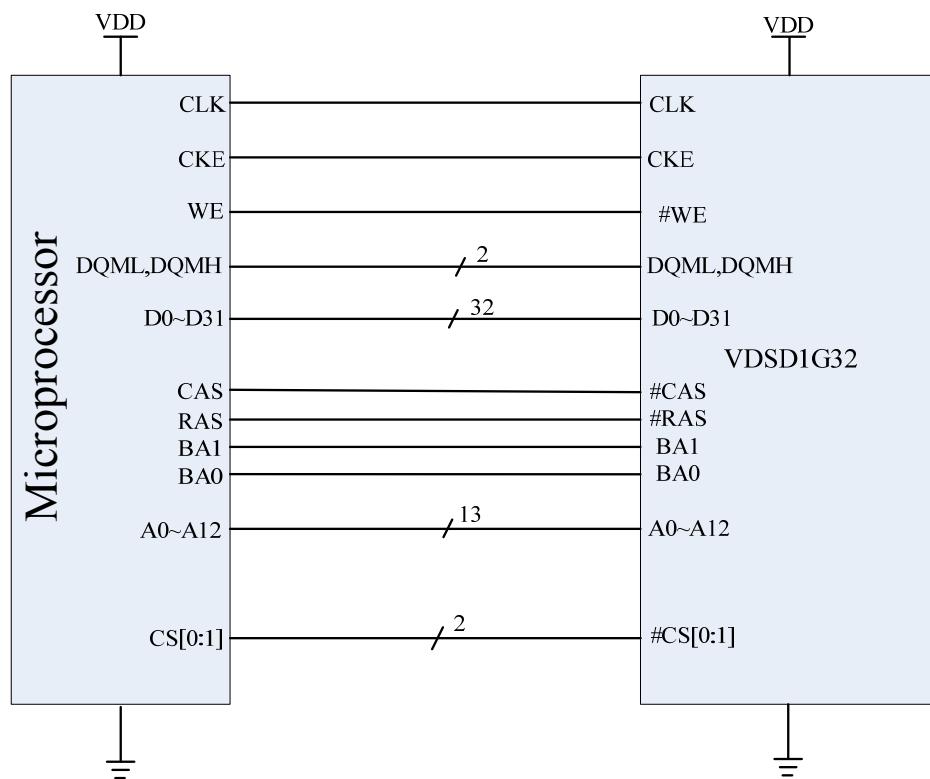
Figure 2 Typical application

7 ORDERING INFORMATION

1	2	3	4	5	6	7	8	9	10	11	12	13
VD	**SD**	**1G**	**32**	**X**	**S**	**70**	**X**	**X**	**2**	**V**	**75**	_

VDIC

SDRAM

Capability: 1Gbit

Bus Width: 32bit

R= Radiation Data Tested;
V= Generic Radiation Data Available

Package: SOP

Pin Quantity: 70 Pin

Temperature: E=0～+70℃; I=-40～+85℃; S=-55~+105℃

Quality: E=Sample; B=Industry; S=Space

Stacking Layer: 2 layers

Power Supply : 3.3V

Frequency: 133MHz

Version: First Version
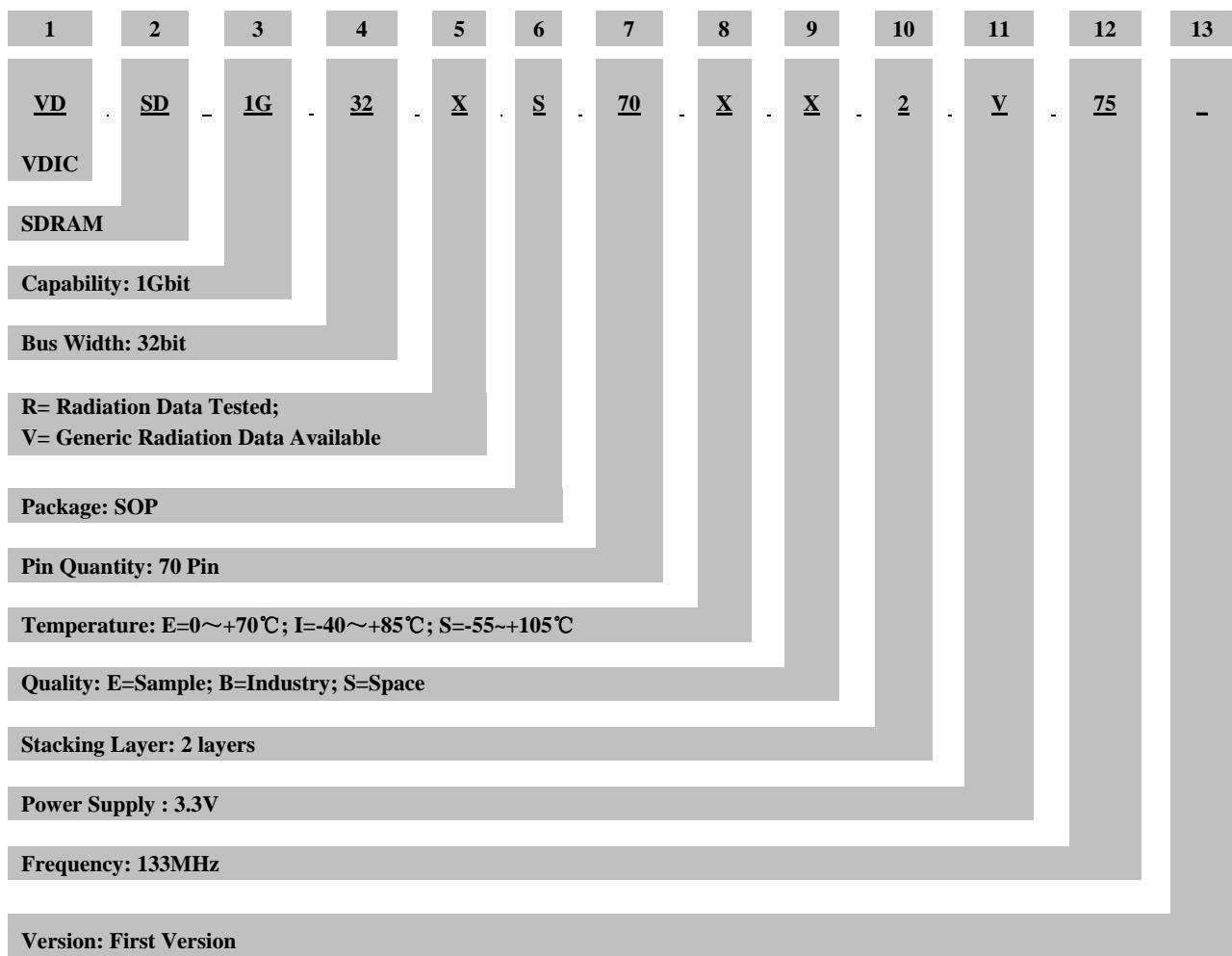
Table 5 Ordering information

Part Numbe	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature （℃）
			TID[1]	SEL[2]	SEU[3]		
VDSD1G32VS70EE2V75	1G	32	-	-	-	SOP70	0~+70
VDSD1G32VS70IB2V75	1G	32	-	-	-	SOP70	-40~+85
VDSD1G32RS70SS2V75	1G	32	50	80	1	SOP70	-55~+105

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[1] TID: Total Dose （Krads(Si)）
[2] SEL: LET Threshold （Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8   PACKAGE DIMENSIONS

TOP VIEW   SIDE VIEW

H/4:1   I/2:1
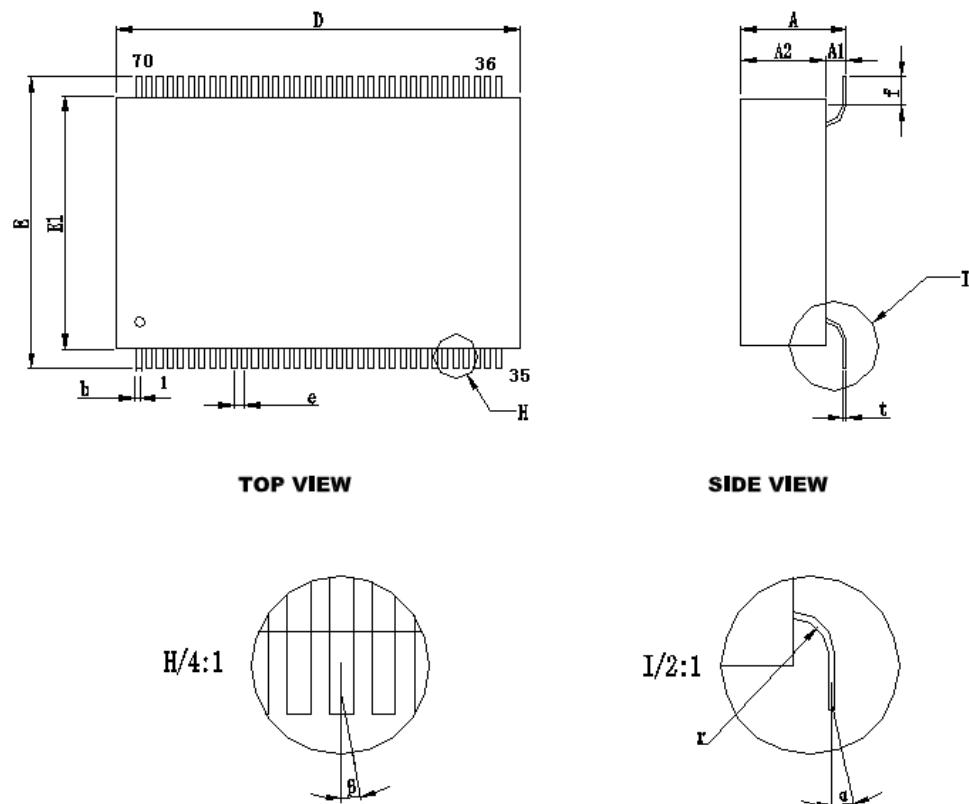
Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Typical	Max
A	6.00	—	6.70
A2	4.80	—	5.40
D	23.80	—	24.20
E	17.40	—	17.80
E1	14.80	—	15.20
f	1.8	—	2.2
b	0.32	—	0.38
e	—	0.635	—
r	1.00	—	1.20
t	0.18	—	0.22

α	—	—	3°
β	—	—	3°

NOTE: 1.Uint: mm
     2. A1= A - A2

9   Pads Designation

It is highly recommended to design pads as below.
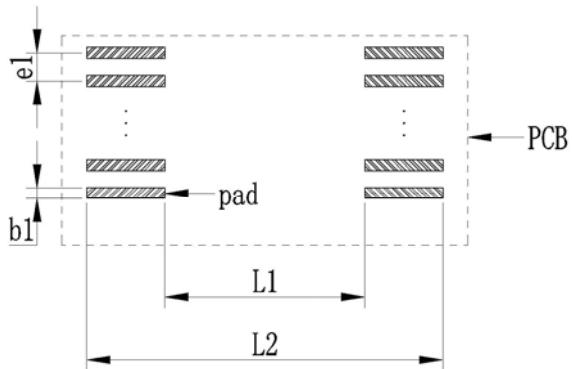
Figure 5 Pads Dimensions

NOTE:

e1: 0.635 mm;

b1: 0.45mm;

L1: 10.4mm;

L2: 18.8mm.

10 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified PIN DESCRIPTIONS
A2	Aug 23,2016	Modified ORDERING INFORMATION
A3	Jan 9,2017	Modified the Truth Table
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Add or reduce chapters
B0	Apr 11,2018	Modified DC characteristics table
B1	Jul 19,2019	Change PACKAGE DIMENSIONS
B2	Mar 25, 2020	Update TID and SEE

B3	April 22, 2021	Add pads designation