VDIC ASYNCHRONOUS STATIC RAM

VDSR16M16XS54XX4V12 USER MANUAL

Version : B3

Document NO.: ORBITA/SIP-VDSR16M16XS54XX4V12-USM-01
Zhuhai Orbita Aerospace Science & Technology Co.，Ltd.

Add: Orbita Tech Park，NO.1 Baisha Road，Tangjia Dong ` an，

Zhuhai，*Guangdong*, China 519080

Tel: +86-756-3391979 Fax: +86-756-3391980

Contents

VDIC-SRAM

HIGH-SPEED 3.3V 1M×16bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR16M16XS54XX4V12 is a high-speed access time, high-density Static Random Access Memory. Manufactured with VDIC Very Dense SIP technology, this SIP module stacks four 4-Mbit SRAM banks employing CMOS process (6-transistor memory cell). It is organized as four independent blocks of 256K x 16bit wide data interface.

Each block can be selected separately with dedicated #CSn.

Low interconnect parasitic capacitance of the stacking technology , by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR16M16XS54XX4V12 is available in 54-pin SOP package.

2 Features

- Single 3.3V±0.3V power supply
- Stack of four 4Mbit SRAM
- Organized as 4 blocks of 256Kx16bit
- Four independent Chip Select, #CS0、#CS1、#CS2、#CS3
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Access time: 15ns
- Max. Operating current: 120mA (Max)
- TTL Standby current: 30mA(Max)
- CMOS standby current: 8mA(Max)
- No clock or timing strobe required
- 54-lead SOP package

3 Block Diagram

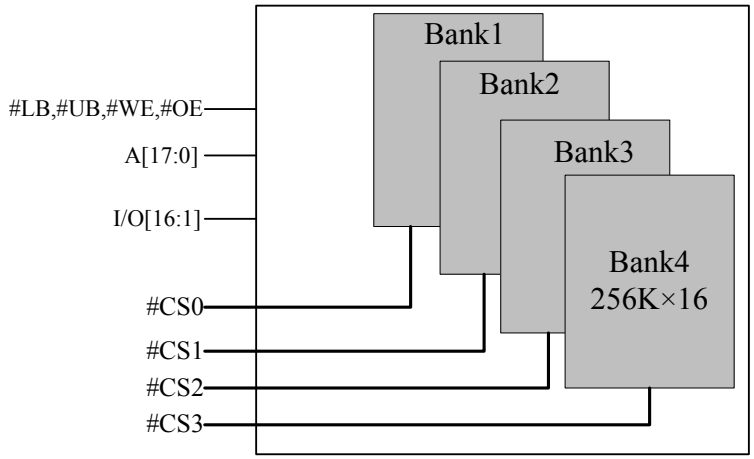

Figure 1 Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
NC	1	54	**#CS3**
NC	2	53	**#CS1**
A0	3	52	**A17**
A1	4	51	**A16**
A2	5	50	**A15**
A3	6	49	**#OE**
A4	7	48	**#UB**
#CS0	8	47	**#LB**
I/O1	9	46	**I/O16**
I/O2	10	45	**I/O15**
I/O3	11	44	**I/O14**
I/O4	12	43	**I/O13**
VCC	13	42	**VSS**
VSS	14	41	**VCC**
I/O5	15	40	**I/O12**
I/O6	16	39	**I/O11**
I/O7	17	38	**I/O10**
I/O8	18	37	**I/O9**
#WE	19	36	**NC**
A5	20	35	**A14**
A6	21	34	**A13**
A7	22	33	**A12**
A8	23	32	**A11**
A9	24	31	**A10**
NC	25	30	**#CS2**
NC	26	29	**NC**
NC	27	28	**NC**

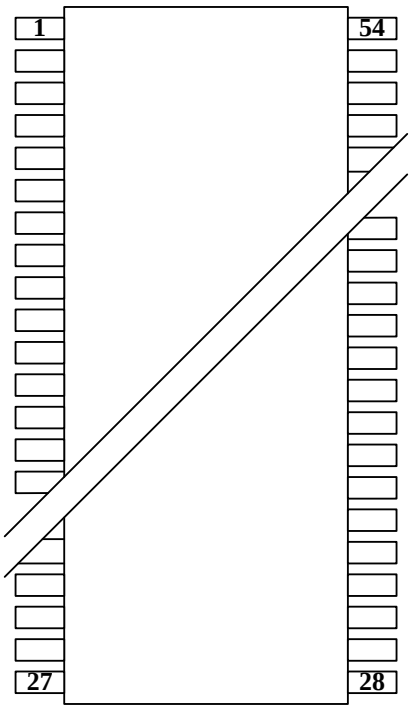

Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0	Chip select	Disables or enables memory bank1 operation
#CS1	Chip select	Disables or enables memory bank 2 operation
#CS2	Chip select	Disables or enables memory bank 3 operation
#CS3	Chip select	Disables or enables memory bank 4 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all banks
#OE	Output enable	Enables data output command to all banks
#UB	Upper byte select	Latches upper bytes data(I/O[16:9]) to all banks
#LB	Lower byte select	Latches lower bytes data (I/O[8:1]) to all banks
I/O1 ~ I/O16	Data input/output	Data inputs/outputs 16-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to +V_{CC}+0.5	V
Power Dissipation	P_D	≤1.0	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input logic high voltage	V_{IH}	2.0	-	V_{cc}+0.5	V
Input logic low voltage	V_{IL}	-0.5	-	0.8	V

5.3 DC Electrical Characteristics Over The Operating

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V, I_{OL}=1mA	-	0.4	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-0.5mA	2.4	-	V

6 Typical Application

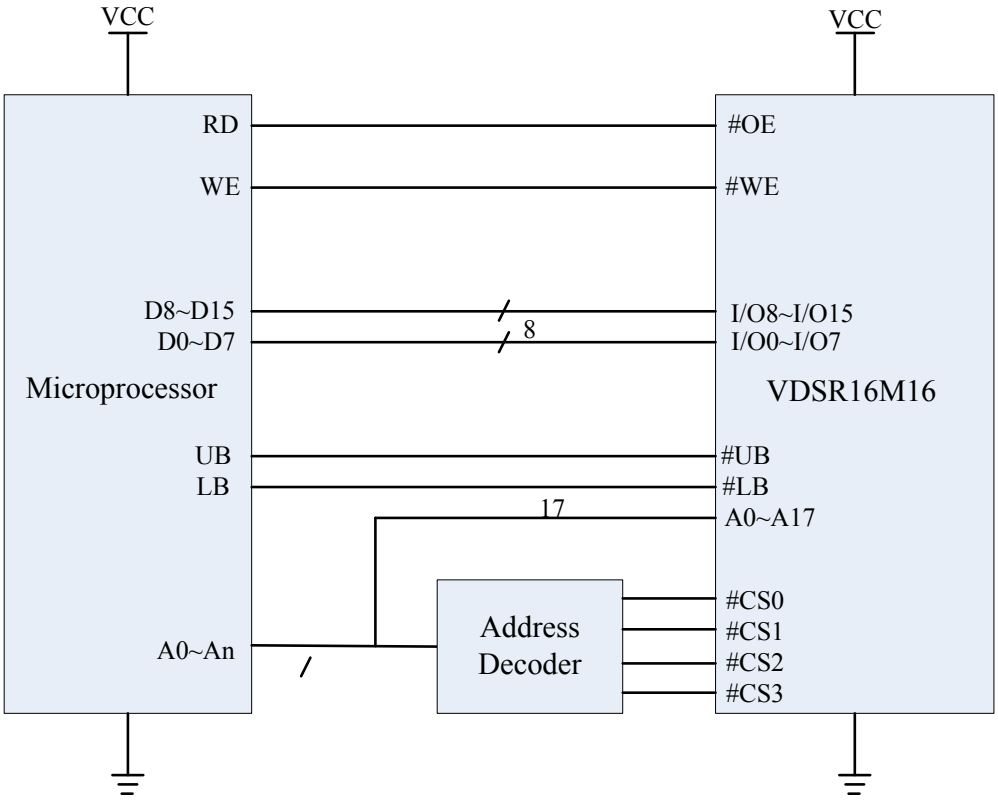

Figure 3 Typical application

7 Ordering Information

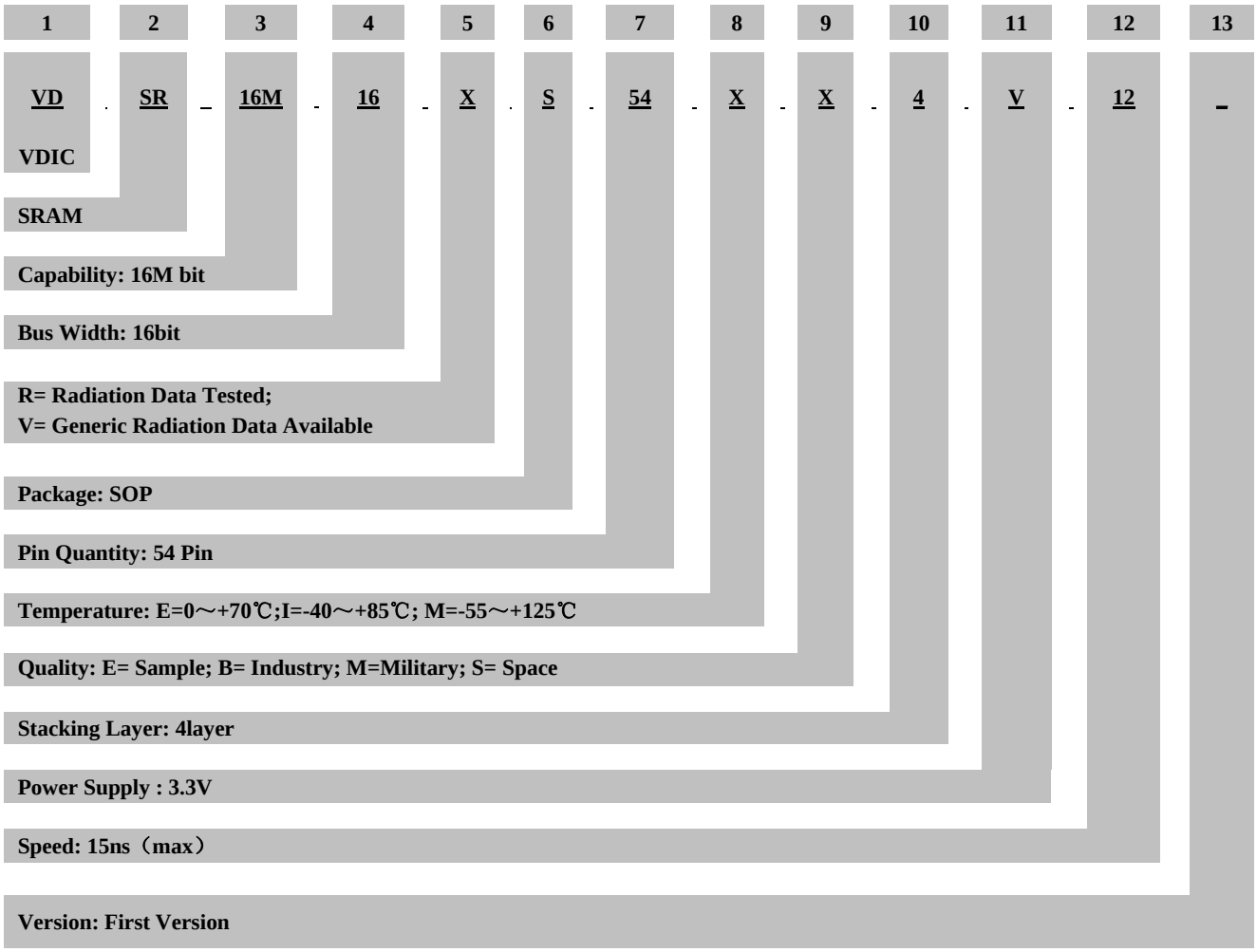

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR16M16VS54EE4V12	16M	16	-	-	-	SOP54	0 ~ + 70
VDSR16M16VS54IB4V12	16M	16	-	-	-	SOP54	-40 ~ + 85
VDSR16M16VS54MM4V12	16M	16	-	-	-	SOP54	-55 ~ + 125
VDSR16M16RS54MS4V12	16M	16	100	> 81.4	< 8.94	SOP54	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（MeV.cm^2/mg）
[3] SEU:SEU Threshold （MeV.cm^2/mg）

8 Package Dimensions

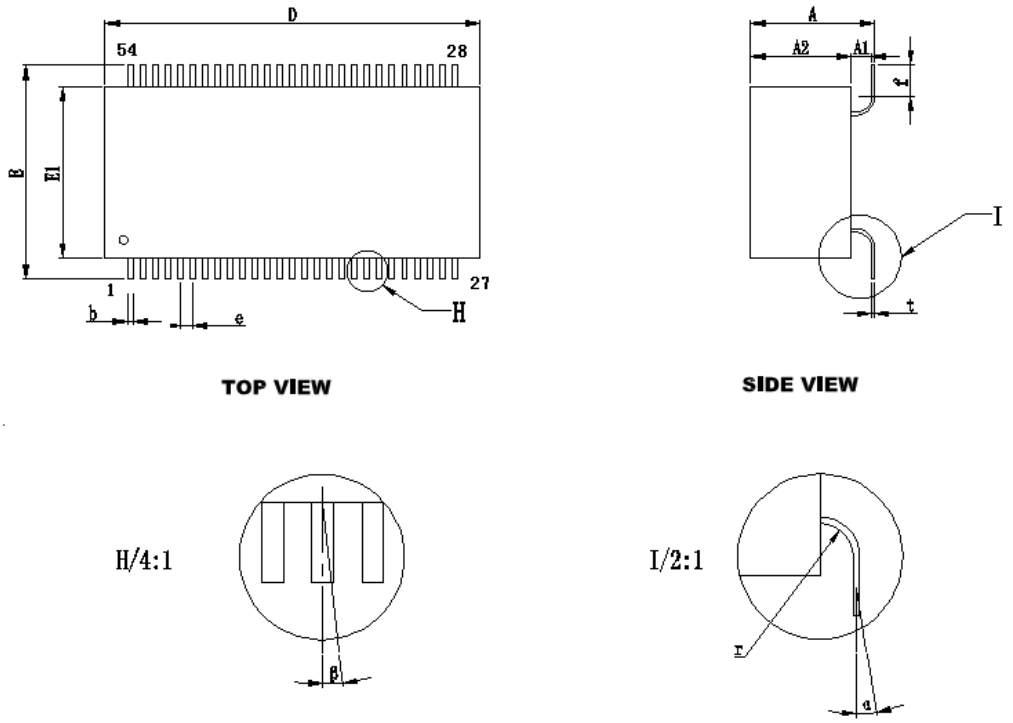

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Typical	Max
A	7.40	—	7.90
A2	6.20	—	6.60
D	23.80	—	24.20
E	13.40	—	13.80
E1	10.80	—	11.20
f	1.80	—	2.20
b	0.32	—	0．38
e	—	0.8	—
r	1.00	—	1.20
t	0.18	—	0.22
α	—	—	3°
β	—	—	3°
NOTE: 1.Uint: mm 2. A1= A - A2			

9 Pads Designation

It is highly recommended to design pads as below.

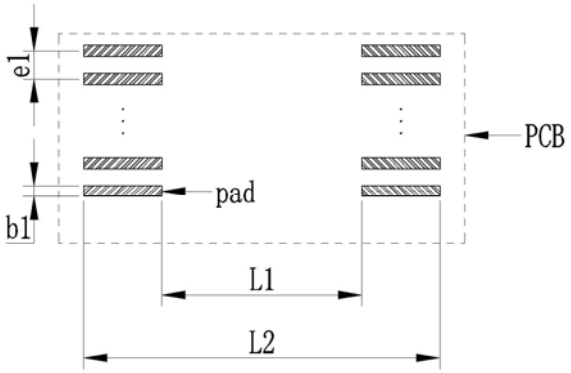

Figure 5 Pads Dimensions

NOTE:

e1: 0.80 mm;

b1: 0.50mm;

L1: 6.4mm;

L2: 14.8mm.

10 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov.15.2017	Modified FEATURES
B0	Apr 13,2018	Add or reduce chapters
B1	Oct 18,2018	Update TID and SEE
B2	Feb 22, 2021	Update SEE
B3	April 22, 2021	Add pads designation