VDIC ASYNCHRONOUS STATIC RAM

VDSR32M32XS68XX8V12-II USER MANUAL

Version : B2

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Contents

VDIC-SRAM

HIGH-SPEED 1M×32bit

ASYNCHRONOUS STATIC RAM

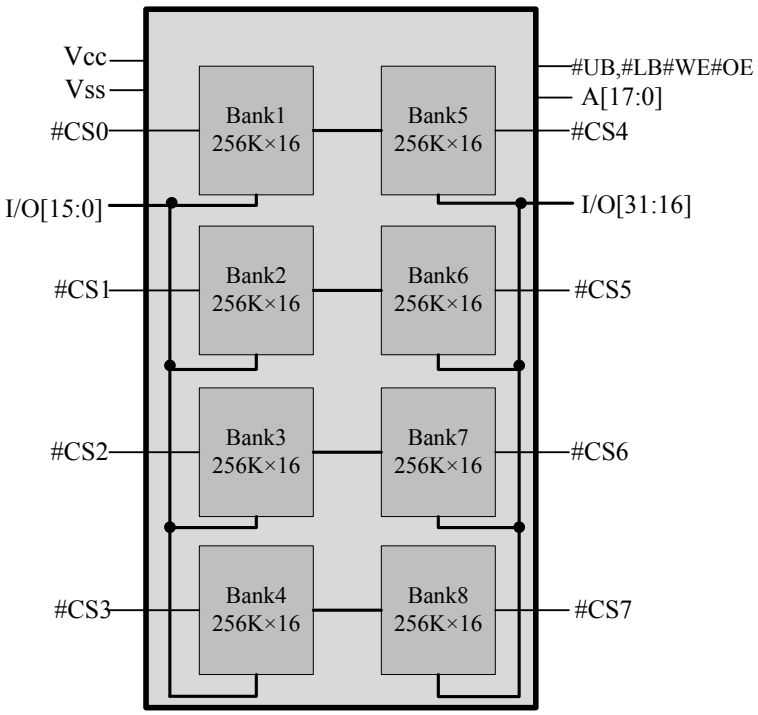
1 Description

The VDSR32M32XS68XX8V12-II is a high-speed access time, high-density Static Random Access Memory containing 33,554,332 bits. Manufactured with VDIC Very Dense SiP technology, this SiP module stacks eight 4-Mbit SRAM dies employing CMOS process (6-transistor memory cell). It is organized as four independent blocks of 256K x 32bit wide data interface. Each block can be selected separately with dedicated #CSn. Low interconnect parasitic capacitance of the stacking technology，by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.
The VDSR32M32XS68XX8V12-II is available in 68-pin SOP package.

2 Features

- Single 3.3V±0.3V power supply
- Stack of eight 4Mbit SRAM
- Organized as 4 blocks of 256K×32bit
- Eight independent Chip Select, #CS0 ,#CS1 ,#CS2,#CS3,#CS4,#CS5,#CS6,#CS7
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Fast Access time: 12ns
- Max. Operating current: 290 mA
- Max. Standby TTL current: 320 mA
- Max. Standby CMOS current: 40mA
- No clock or timing strobe required
- CenterVcc and Vss type pin out
- 68-lead SOP Type II package

3 Block Diagram



(All other signals are common to the eight memories)

Figure 1: Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
#CS5	1	68	**#CS7**
I/O18	2	67	**#CS3**
I/O17	3	66	**I/O28**
I/O16	4	65	**I/O29**
#CS1	5	64	**I/O30**
#CS4	6	63	**I/O31**
A0	7	62	**A17**
A1	8	61	**A16**
A2	9	60	**A15**
A3	10	59	**#OE**
A4	11	58	**#UB**
#CS0	12	57	**#LB**
I/O0	13	56	**I/O15**
I/O1	14	55	**I/O14**
I/O2	15	54	**I/O13**
I/O3	16	53	**I/O12**
VCC	17	52	**VSS**
VSS	18	51	**VCC**
I/O4	19	50	**I/O11**
I/O5	20	49	**I/O10**
I/O6	21	48	**I/O9**
I/O7	22	47	**I/O8**
#WE	23	46	**#CS2**
A5	24	45	**A14**
A6	25	44	**A13**
A7	26	43	**A12**
A8	27	42	**A11**
A9	28	41	**A10**
I/O23	29	40	**I/O24**
I/O22	30	39	**I/O25**
I/O21	31	38	**I/O26**
I/O20	32	37	**I/O27**
I/O19	33	36	**#CS6**
NC	34	35	**NC**

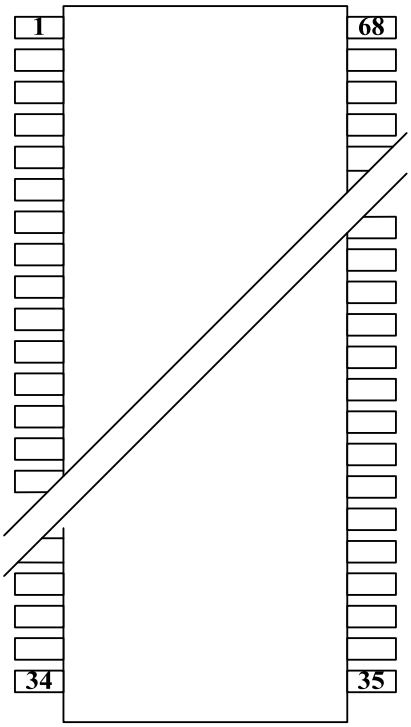


Figure 1 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0 ~ #CS7	Chip select	Disables or enables memory bank1 ~ bank8 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all banks
#OE	Output enable	Enables data output command to all banks
#UB	Upper byte select	Latches upper bytes data(I/O[15:8],I/O[31:24]) to all banks
#LB	Lower byte select	Latches lower bytes data (I/O[7:0],I/O[23:16]) to all banks

I/O0 ~ I/O31	Data input/output	Data inputs/outputs 32-bit wide bus : Data I/O0 to I/O15 activated from bank 1 ~bank4 and Data I/O16 to I/O31 activated from bank 5 ~ bank 8.
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

1.1. Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to V_{CC}+0.5	V
Power Dissipation	P_D	2	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

1.2. Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{CC}+0.5	V
Input low voltage	V_{IL}	-0.5	——	0.8	V

1.3. DC Electrical Characteristics Over The Operating

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V, I_{OL}=1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-0.5mA	2.4	——	V

6 Typical Application

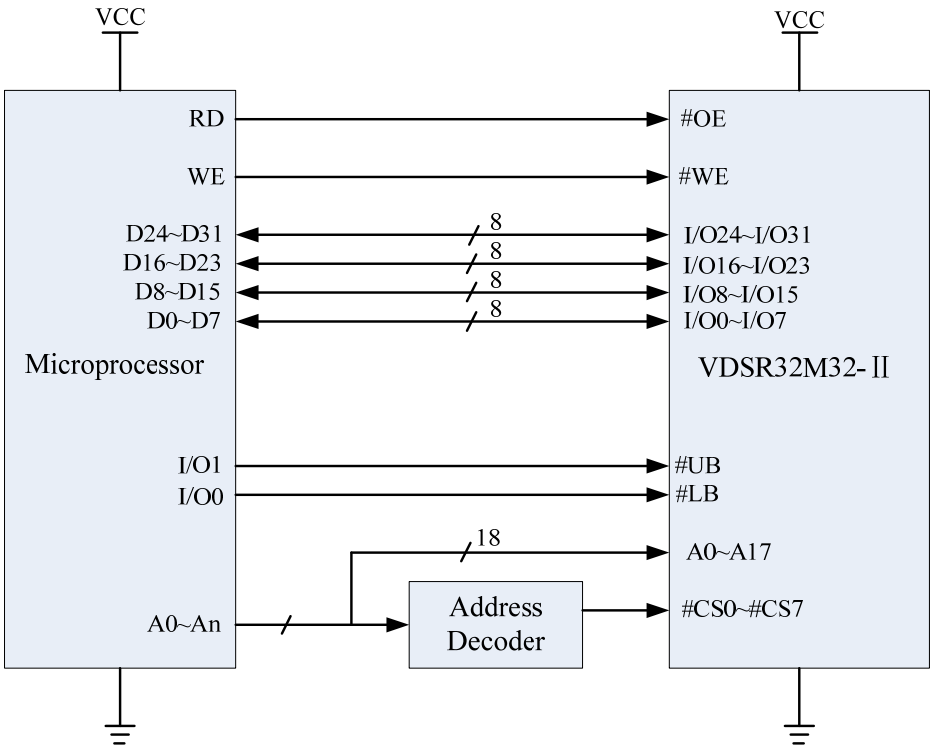


Figure 2 Typical application

7 Ordering Information

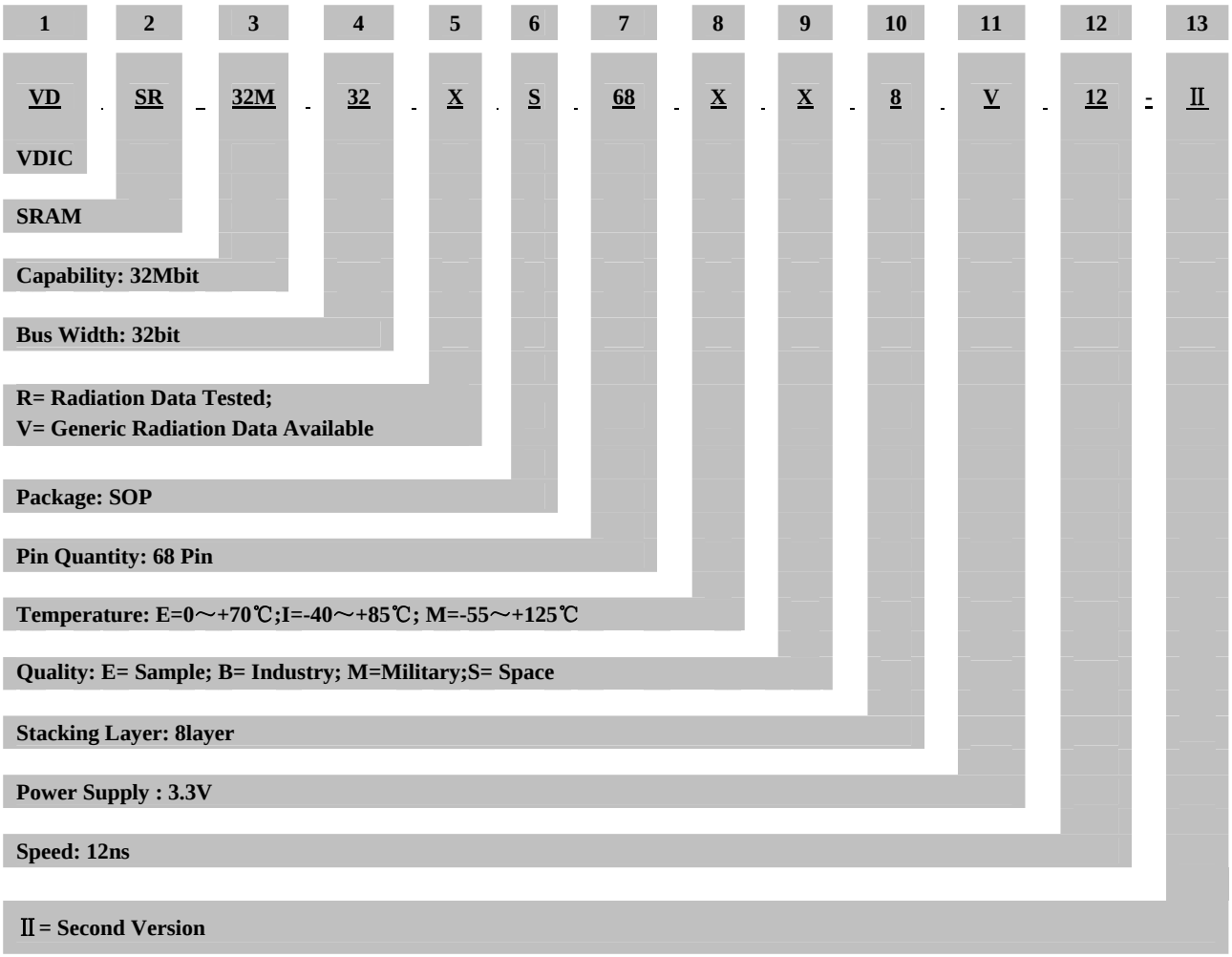


Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR32M32VS68EE8V12-II	32M	32	-	-	-	SOP68	0 ~ + 70
VDSR32M32VS68IB8V12-II	32M	32	-	-	-	SOP68	-40 ~ + 85
VDSR32M32VS68MM8V12-II	32M	32	-	-	-	SOP68	-55 ~ + 125
VDSR32M32RS68MS8V12-II	32M	32	> 100	> 75	> 0.9	SOP68	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 Package Dimensions

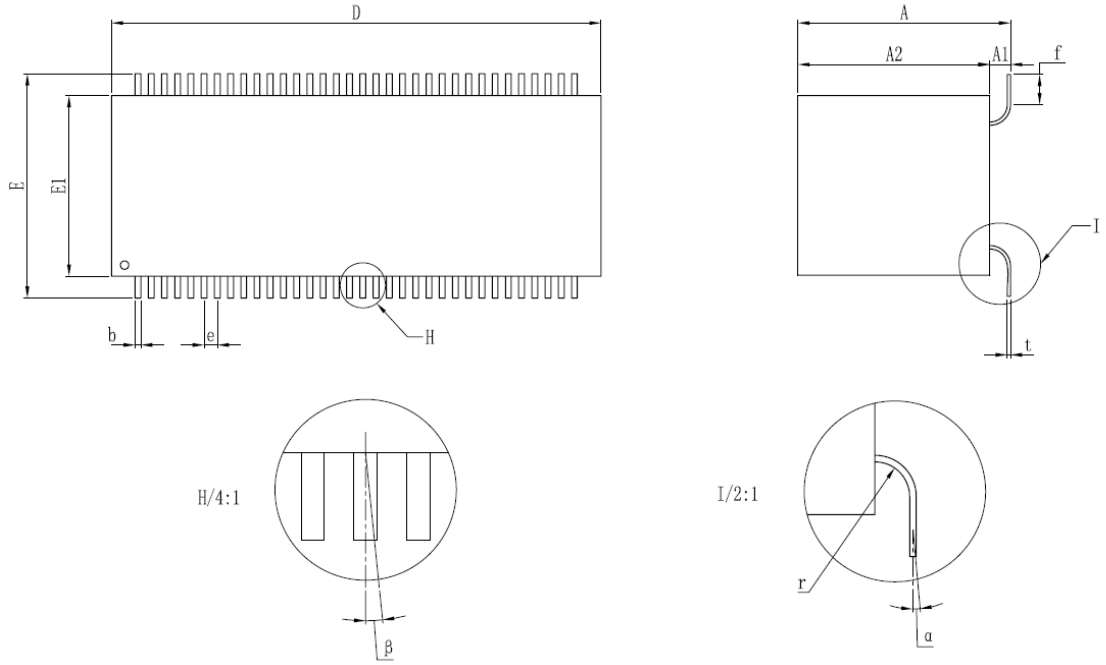


Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.60	13.20
A2	11.40	11.90
D	29.50	29.90
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov.15.2017	Modified FEATURES
B0	Apr 13,2018	Add or reduce chapters
B1	Oct 18,2018	Revising pin descriptions
B2	Apr 10,2019	Modified Typical Application
B3	Mar 21,2020	Update TID and SEE