VDIC ASYNCHRONOUS STATIC RAM

VDSR20M40XS84XX6V12 USER MANUAL

Version : B6

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VDIC-SRAM

HIGH-SPEED 512K x 40bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR20M40XS84XX6V12 is a high-speed access time, high-density Static Random Access Memory with 20Mbit. Manufactured with VDIC Very Dense SIP technology, this die stacks six SRAM dies employing CMOS process (6-transistor memory cell). It is organized as two independent blocks of 256Kx40bit wide data interface .Each block can be selected separately with dedicated #CSn.

Low interconnect parasitic capacitance of the stacking technology, by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR20M40XS84XX6V12 is available in a 84-pin SOP package.

2 Features

- Single 3.3V± 0.3V power supply
- Six Dies with three independent Selects: #CS0/#CS1/ #CS2/ #CS3
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Access time: 15ns
- Max. Operating current: 265 mA
- Standby current: 40 mA
- No clock or timing strobe required
- 84-lead SOP Type II package

3 Block Diagram

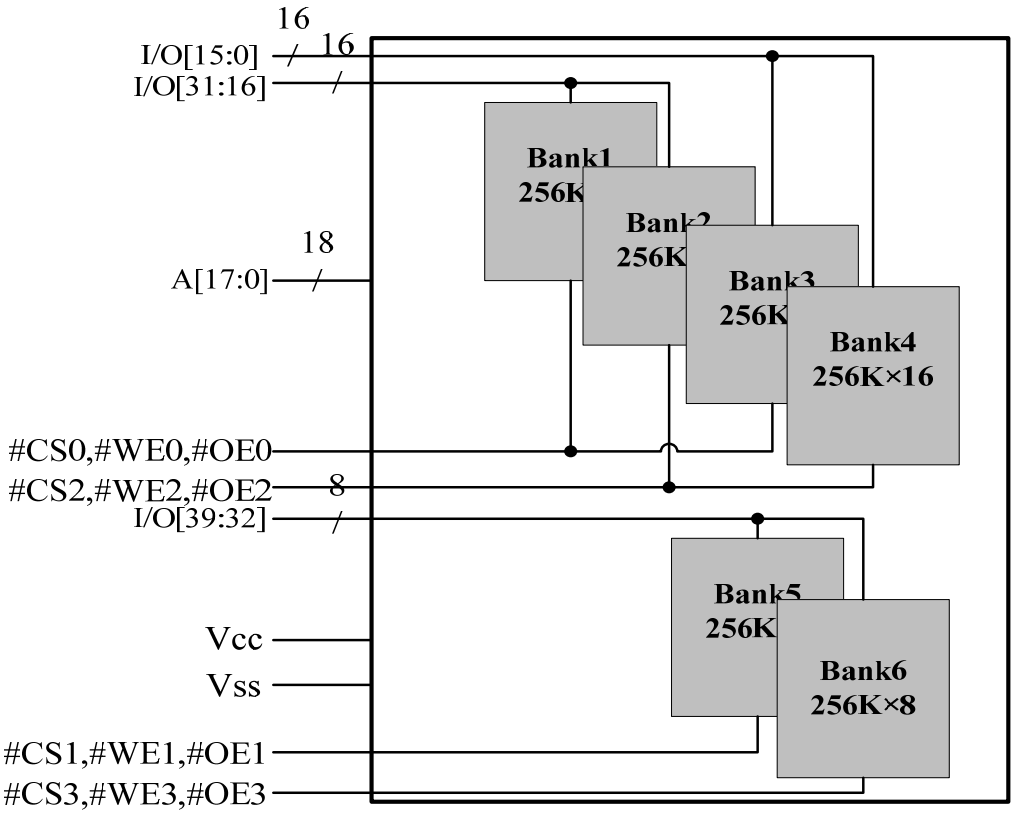

Figure 1: Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin Id
A9	1	84	**A0**
A8	2	83	**A1**
A7	3	82	**A2**
A6	4	81	**A3**
A5	5	80	**A4**
I/O7	6	79	**I/O0**
I/O23	7	78	**I/O16**
I/O39	8	77	**I/O32**
I/O6	9	76	**I/O1**
I/O22	10	75	**I/O17**
I/O38	11	74	**I/O33**
I/O5	12	73	**I/O2**
I/O21	13	72	**I/O18**
I/O37	14	71	**I/O34**
I/O4	15	70	**I/O3**
I/O20	16	69	**I/O19**
I/O36	17	68	**I/O35**
VSS	18	67	**NC**
VSS	19	66	**#CS0**
VSS	20	65	**#CS1**
VSS	21	64	**#CS2**
VSS	22	63	**#CS3**
NC	23	62	**NC**
NC	24	61	**#WE3**
VCC	25	60	**#WE2**
VCC	26	59	**#WE1**
VCC	27	58	**#WE0**
VCC	28	57	**#OE0**
VCC	29	56	**#OE1**
I/O27	30	55	**#OE2**
I/O11	31	54	**#OE3**
I/O26	32	53	**I/O28**
I/O10	33	52	**I/O12**
I/O25	34	51	**I/O29**
I/O9	35	50	**I/O13**
I/O24	36	49	**I/O30**
I/O8	37	48	**I/O14**
A14	38	47	**I/O31**
A13	39	46	**I/O15**
A12	40	45	**A15**
A11	41	44	**A16**
A10	42	43	**A17**

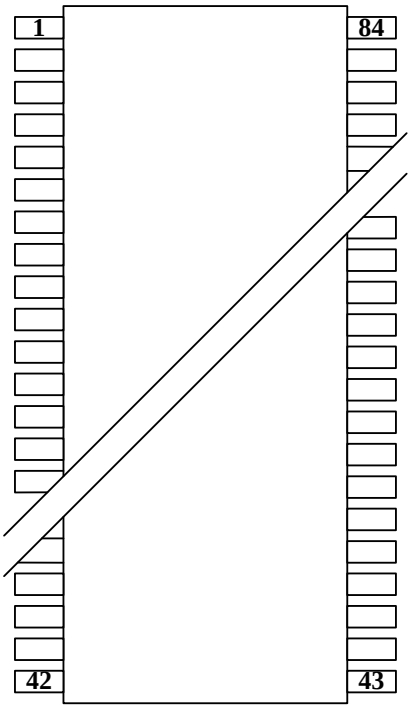

Figure 1 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0	Die select	Disables or enables memory bank1 and bank3 operation
#CS1	Die select	Disables or enables memory bank 5 operation
#CS2	Die select	Disables or enables memory bank 2 and bank 4 operation
#CS3	Die select	Disables or enables memory bank 6 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all memory banks
#OE	Output enable	Enables data output command to all memory banks
I/O0~ I/O39	Data input/output	Data inputs/outputs 40-bit wide bus
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to 4.6	V
Power Dissipation	P_D	< 3.0	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{CC}+0.3	V
Input low voltage	V_{IL}	-0.3	——	0.8	V

5.3 DC Electrical Characteristics

Table 4 DC characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V, I_{OL}=1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-0.5mA	2.4	——	V

6 Typical Application

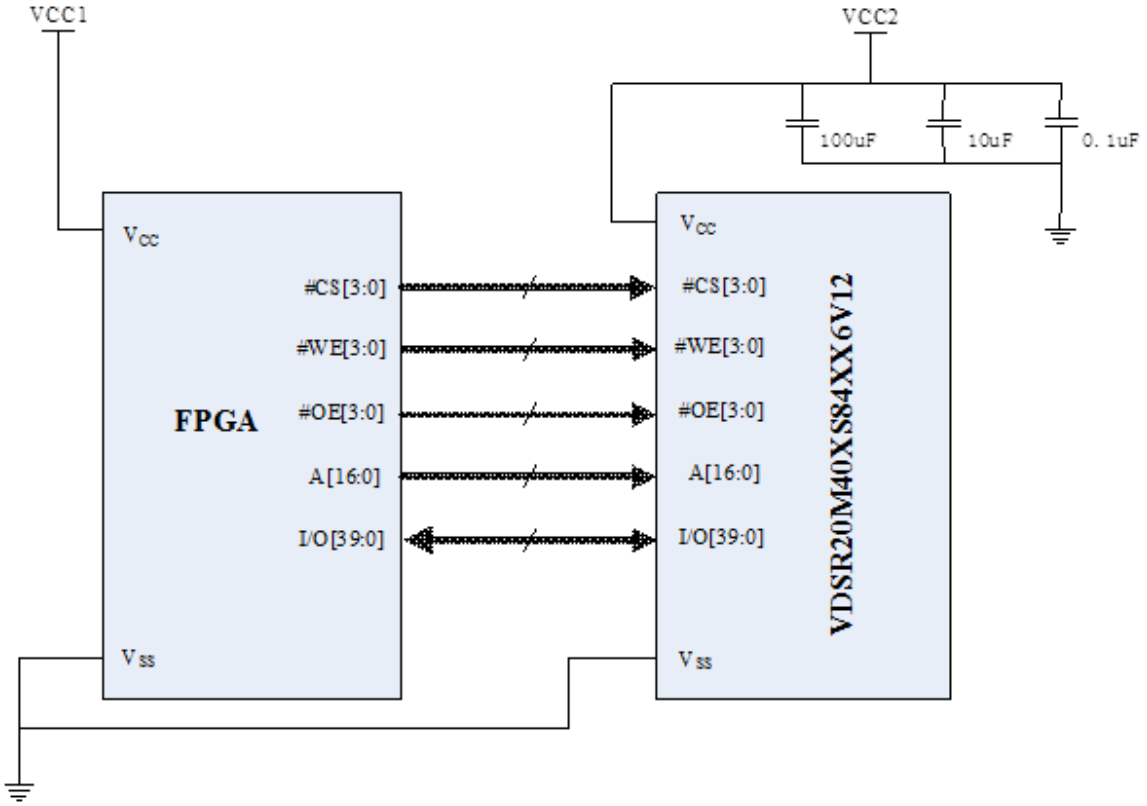

Figure 2 Typical application

7 Ordering Information

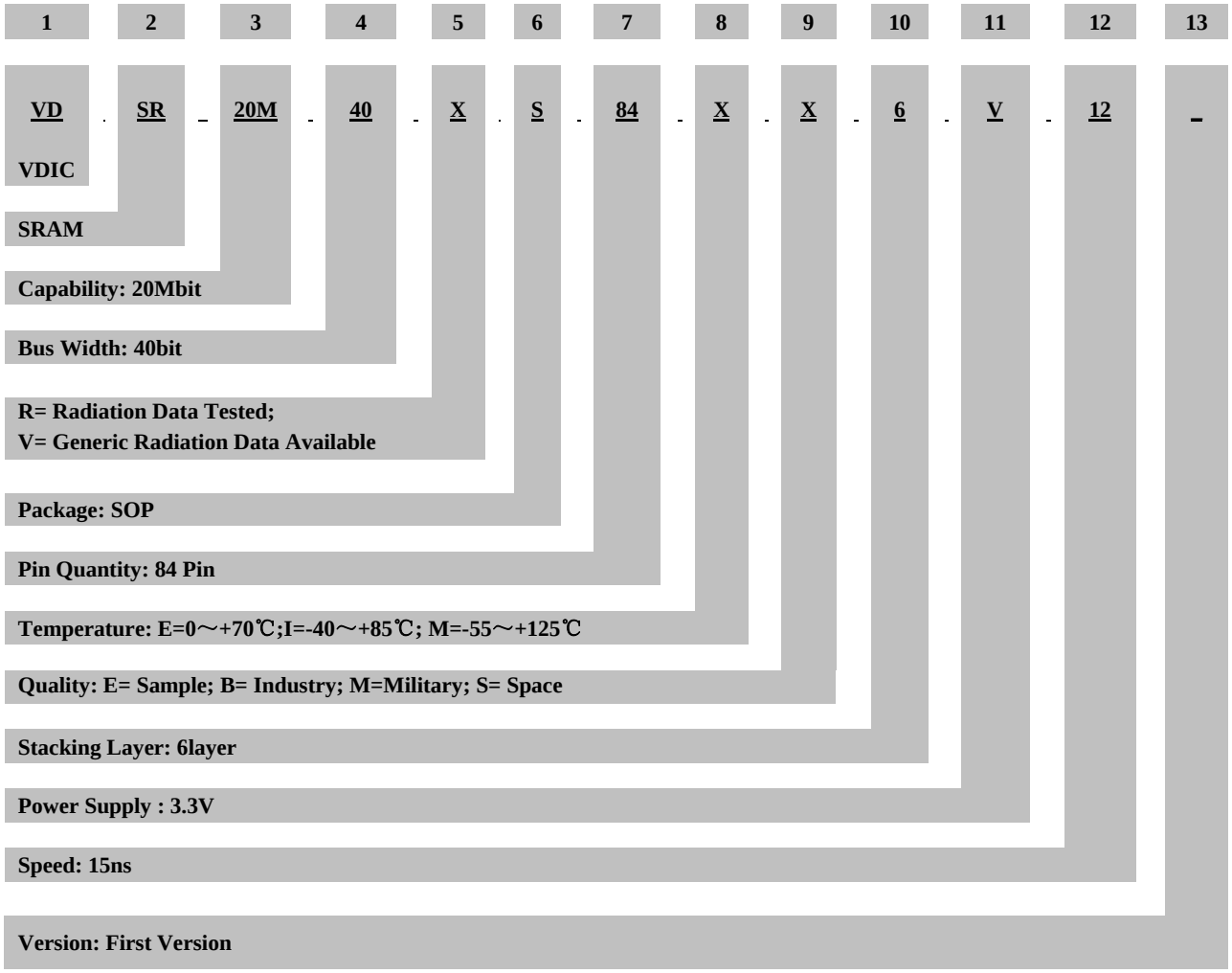

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR20M40VS84EE6V12	20M	40	-	-	-	SOP84	0 ~ + 70
VDSR20M40VS84IB6V12	20M	40	-	-	-	SOP84	-40 ~ + 85
VDSR20M40VS84MM6V12	20M	40	-	-	-	SOP84	-55 ~ + 125
VDSR20M40RS84MS6V12	20M	40	≥100	≥75	≥0.9	SOP84	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm^2/mg）
[3] SEU:SEU Threshold （Mev.cm^2/mg）

8 Package Dimensions

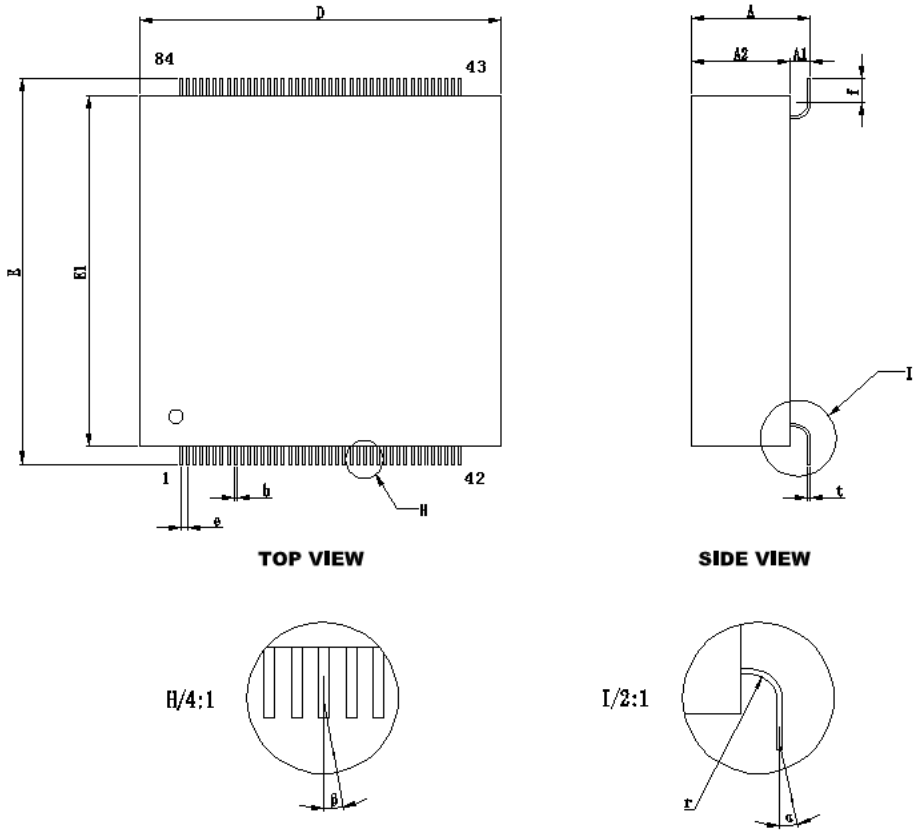

Figure 3 Package dimensions

Table 6 Dimensions information

	最小值	公称值	最大值
A	8.30	—	9.00
A2	7.10	—	7.70
D	26.80	—	27.20
E	28.50	—	28.90
E1	25.90	—	26.30
f	1.50	—	2.00
b	0.22	—	0.28
e	—	0.508	—
r	0.80	—	1.20
t	0.18	—	0.22
α	—	—	3℃

	最小值	公称值	最大值
β	—	—	3℃

9 Pads Designation

It is highly recommended to design pads as below.

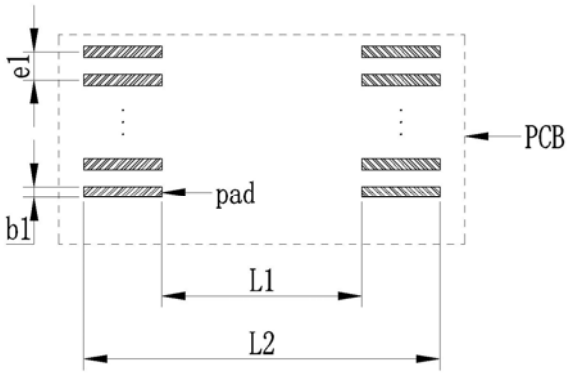

Figure 5 Pads Dimensions

NOTE:

e1: 0.508 mm;

b1: 0.30mm;

L1: 21.9mm;

L2: 29.9mm.

10 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description
A0	Nov 3,2015	Initial Release
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the PACKAGE DIMENSIONS
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov.15.2017	Modified FEATURES
B0	Apr 13,2018	Add or reduce chapters
B1	Oct 18,2018	Revising pin descriptions

B2	JAN 17, 2020	Operating temperature -55～+125℃ instead of -55～+95℃，typical application updated.
B3	Mar 21,2020	Update TID and SEE
B4	April 22, 2021	Add pads designation
B5	July 27, 2021	Update pin space
B6	September 2, 2021	Update TID 100 and SEE 75 & 0.9