VDIC ASYNCHRONOUS STATIC RAM

VDSR16M32XS64XX4V12 USER MANUAL

Version: B1

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VDIC-SRAM

HIGH-SPEED 512K× 32bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR16M32XS64XX4V12 is a high-speed access time, high-density Static Random Access Memory containing 16,777,216 bits. Manufactured with VDIC Very Dense SiP technology, this SiP module stacks four 4-Mbit SRAM dies employing CMOS process (6-transistor memory cell). It is organized as two independent blocks of 512K x 32bit wide data interface.

Each block can be selected separately with dedicated #CS0、#CS1.

Low interconnect parasitic capacitance of the stacking technology , by reducing the connection length, allows this SRAM module to be useful for a variety of high bandwidth, high performance and high density memory system applications.

The VDSR16M32XS64XX4V12 is available in 64-pin SOP package.

2 Features

- Single 3.3V±0.3V power supply
- Fast Access time: 15ns
- Stack of four 4Mbit SRAM
- Organized as 2 blocks of 256Kx32bit
- Two independent Chip Select, #CS0 and #CS1
- All inputs and outputs directly TTL compatible
- Equal Access and Cycle times
- Operating current: 320 mA (Max).
- TTL Standby current: 240 mA(typ)
- CMOS Standby current: 40 mA(typ)
- No clock or timing strobe required
- Center Vcc and Vss type pin out

3 Block Diagram

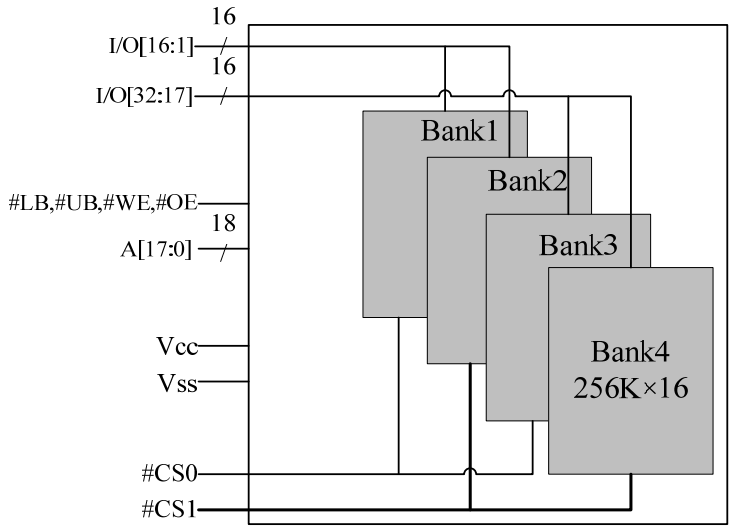

Figure 1: Block diagram

4 Pin Descriptions

Pin Id	Pin #		Pin #	Pin Id
I/O19	1		64	**NC**
I/O18	2		63	**I/O29**
I/O17	3		62	**I/O30**
#CS1	4		61	**I/O31**
NC	5		60	**I/O32**
A0	6		59	**A17**
A1	7		58	**A16**
A2	8		57	**A15**
A3	9		56	**#OE**
A4	10		55	**#UB**
#CS0	11		54	**#LB**
I/O1	12		53	**I/O16**
I/O2	13		52	**I/O15**
I//O3	14		51	**I/O14**
I/O4	15		50	**I/O13**
VCC	16		49	**VSS**
VSS	17		48	**VCC**
I/O5	18		47	**I/O12**
I/O6	19		46	**I/O11**
I/O7	20		45	**I/O10**
I/O8	21		44	**I/O9**
#WE	22		43	**NC**
A5	23		42	**A14**
A6	24		41	**A13**
A7	25		40	**A12**
A8	26		39	**A11**
A9	27		38	**A10**
I/O24	28		37	**I/O25**
I/O23	29		36	**I/O26**
I/O22	30		35	**I/O27**
I/O21	31		34	**I/O28**
I/O20	32		33	**NC**

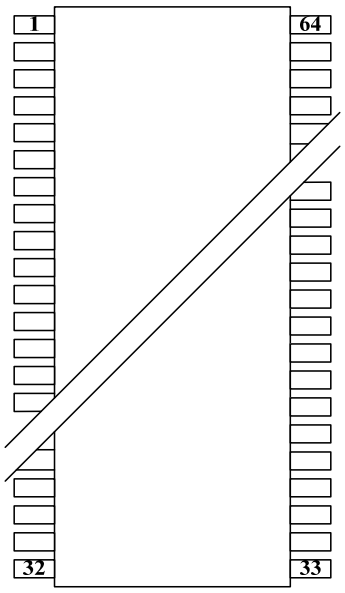

Figure 1 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0	Chip select	Disables or enables memory bank1 and bank 3 operation
#CS1	Chip select	Disables or enables memory bank 2 and bank 4 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all banks
#OE	Output enable	Enables data output command to all banks
#UB	Upper byte select	Latches upper bytes data(I/O[16:9],I/O[32:25]) to all banks
#LB	Lower byte select	Latches lower bytes data (I/O[8:1],I/O[24:17]) to all banks
I/O1 ~ I/O32	Data input/output	Data inputs/outputs 32-bit wide bus : Data I/O1 to I/O16 activated from dies 1 and 2 and Data I/O16 to I/O32 activated from dies 3 and 4
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Command Operation

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to +V_{CC}+0.5	V
Power Dissipation	P_D	1.5	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.0	——	V_{CC}+0.5	V
Input low voltage	V_{IL}	-0.5	——	0.8	V

5.3 DC Characteristics

Table 4 DC characteristics

PARAMETERS	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V_{OL}	V_{CC}=3.6V, I_{OL}=1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{CC}=3.0V, I_{OH}=-0.5mA	2.4	——	V

6 Typical Application

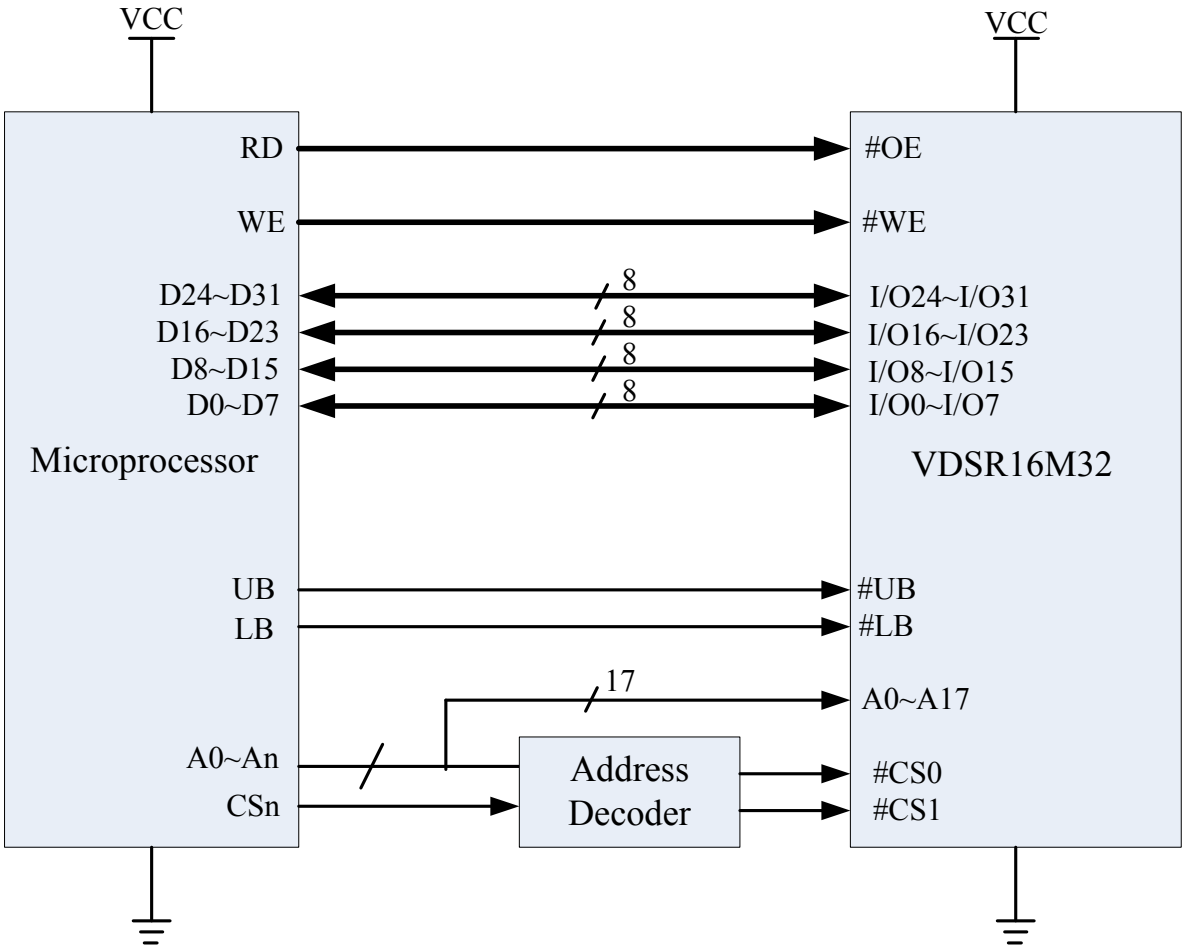

Figure 2 Typical application

7 Ordering Information

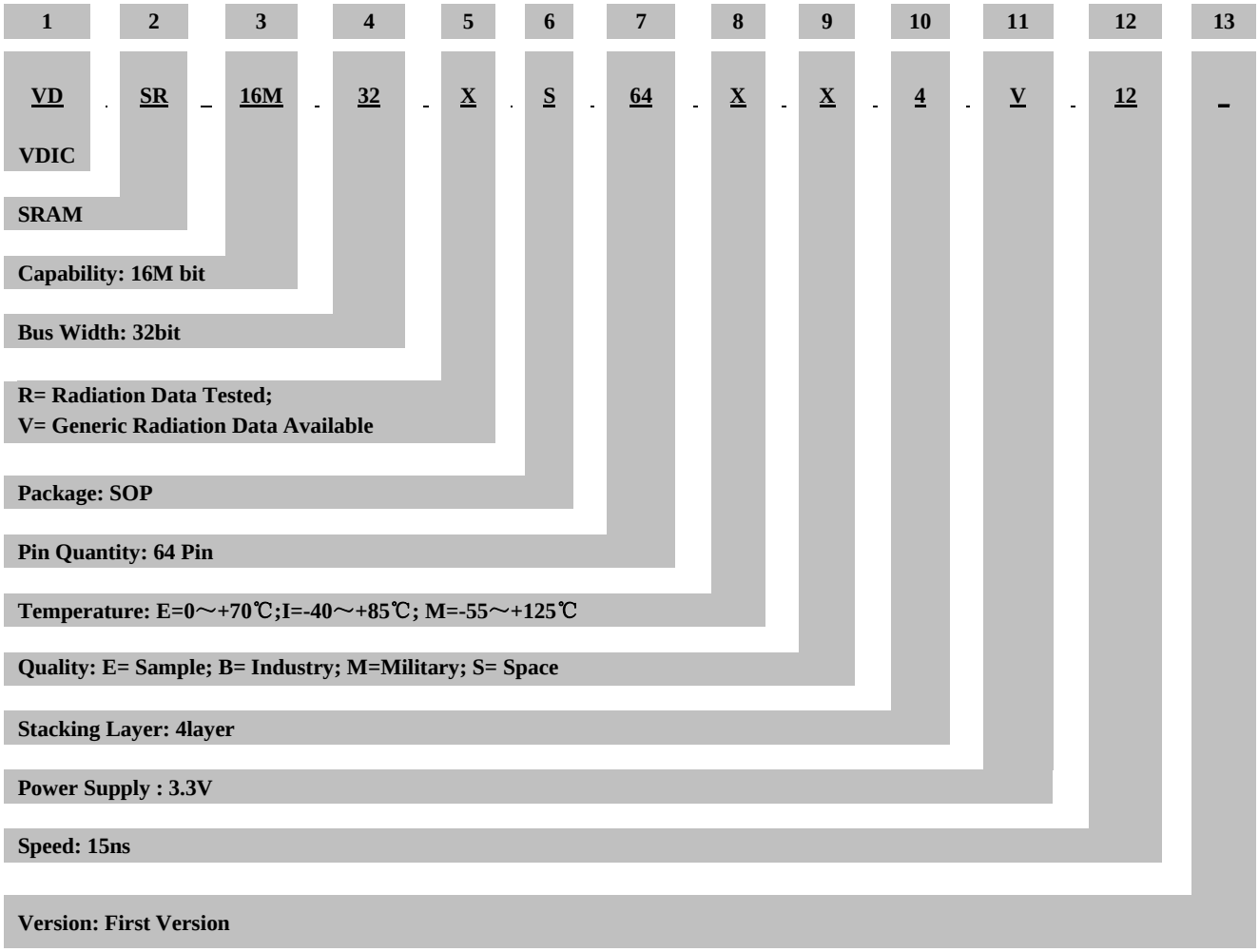

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR16M32VS64EE4V12	16M	32	-	-	-	SOP64	0 ~ + 70
VDSR16M32VS64IB4V12	16M	32	-	-	-	SOP64	-40 ~ + 85
VDSR16M32VS64MM4V12	16M	32	-	-	-	SOP64	-55 ~ + 125
VDSR16M32RS64MS4V12	16M	32	100	>76.5	1.7	SOP64	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 Package Dimensions

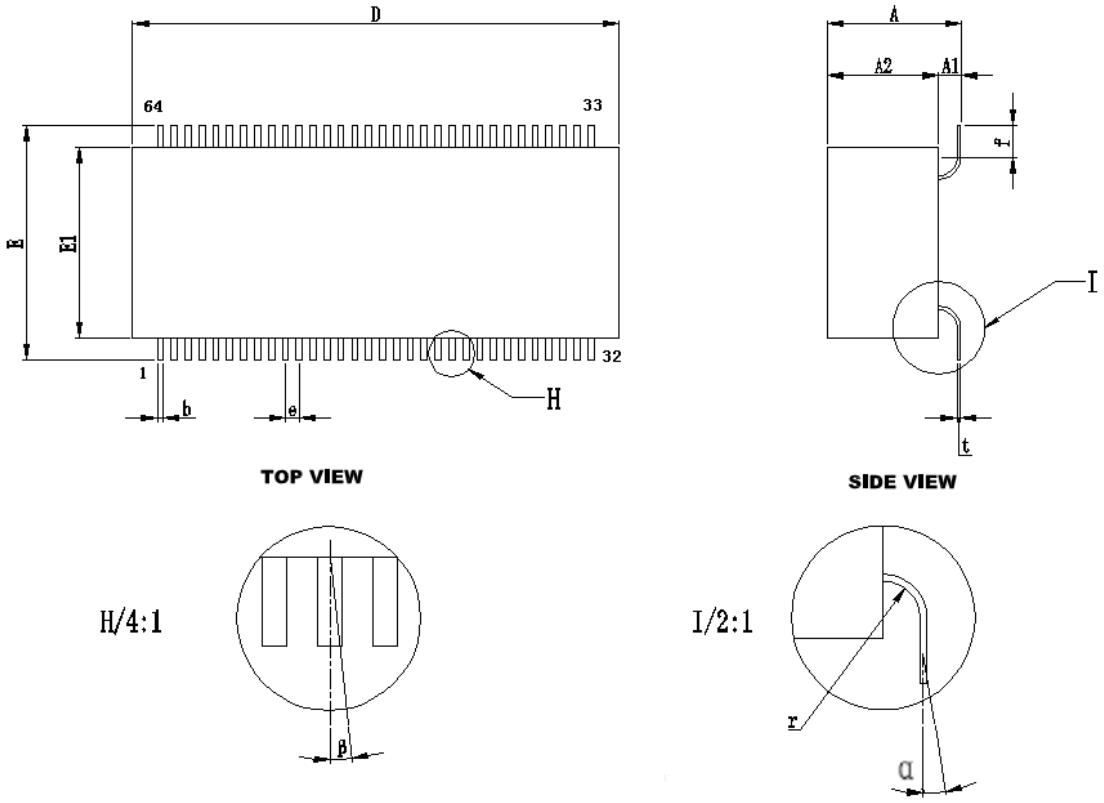

Figure 3 Package dimensions

Table 6 Dimensions information

	Min	Typical	Max
A	7.40	—	7.90
A2	6.20	—	6.60
D	27.80	—	28.20
E	13.40	—	13.80
E1	10.80	—	11.20
f	1.80	—	2.20
b	0.32	—	0．38
e	—	0.8	—
r	1.00	—	1.20
t	0.18	—	0.22
α	—	—	3°
β	—	—	3°
NOTE: 1.Uint: mm 2. A1= A - A2			

9 Pads Designation

It is highly recommended to design pads as below.

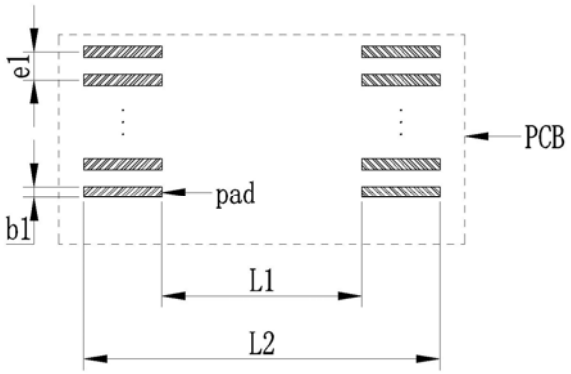

Figure 5 Pads Dimensions

NOTE:

e1: 0.80 mm;

b1: 0.50mm;

L1: 6.4mm;

L2: 14.8mm.

10 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Apr 13,2018	Modified the PACKAGE DIMENSIONS
B0	Oct 18,2018	Revising pin descriptions
B1	April 22, 2021	Add pads designation