VDIC ASYNCHRONOUS STATIC RAM

VDSR8M16XS54XX2C12 USER MANUAL

Version : B0

Document NO.: ORBITA/SIP-VDSR8M16XS54XX2C12-USM-01
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VDIC-SRAM

HIGH-SPEED 512K× 16bit

ASYNCHRONOUS STATIC RAM

1 Description

The VDSR8M16XS54XX2C12 is a high-speed highly integrated Static Random Access Memory containing 8.388.608 bits. It is organized with two banks of 4Mbit.

Each bank has a16-bit interface and is selected with specific #CS.

It is particularly well suited for use in high reliability high performance and high density system applications, such as solid state mass recorder, server or workstation.

The VDSR8M16XS54XX2C12 is packaged in a 54 pin SOP.

2 Features

- Single 5.0V±0.5V power supply
- FastAccess Time: 12, 15, or20ns.
- Single5.0V+/- 10% power supply.
- PowerDissipation:
- Standby 80mA
- Operating 180mA(Max.)
- TTL Compatible Input and Outputs.
- Fully Static Operation
- No clock or Refresh required.
- Three State Outputs.
- CenterPower/Ground Pin Configuration.
- Die control: #CS0, #CS1, chip select.
- Available with screening option for high reliability application
- (Space, etc...).

3 Block Diagram

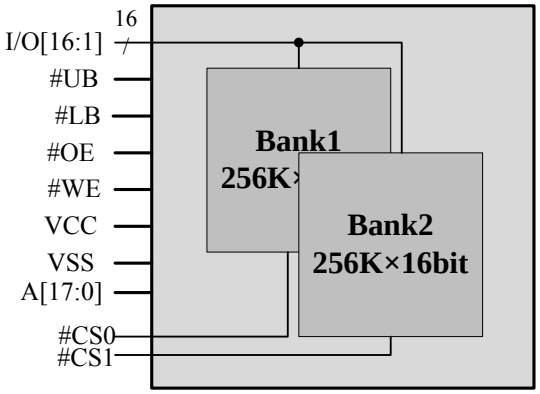

Figure 1 Block diagram

4 Pin Configurations

Pin Id	Pin #		Pin #	Pin Id
NC	1		54	**NC**
NC	2		53	**#CS1**
A0	3		52	**A17**
A1	4		51	**A16**
A2	5		50	**A15**
A3	6		49	**#OE**
A4	7		48	**#UB**
#CS0	8		47	**#LB**
I/O1	9		46	**I/O16**
I/O2	10		45	**I/O15**
I/O3	11		44	**I/O14**
I/O4	12		43	**I/O13**
VCC	13		42	**VSS**
VSS	14		41	**VCC**
I/O5	15		40	**I/O12**
I/O6	16		39	**I/O11**
I/O7	17		38	**I/O10**
I/O8	18		37	**I/O9**
#WE	19		36	**NC**
A5	20		35	**A14**
A6	21		34	**A13**
A7	22		33	**A12**
A8	23		32	**A11**
A9	24		31	**A10**
NC	25		30	**NC**
NC	26		29	**NC**
NC	27		28	**NC**

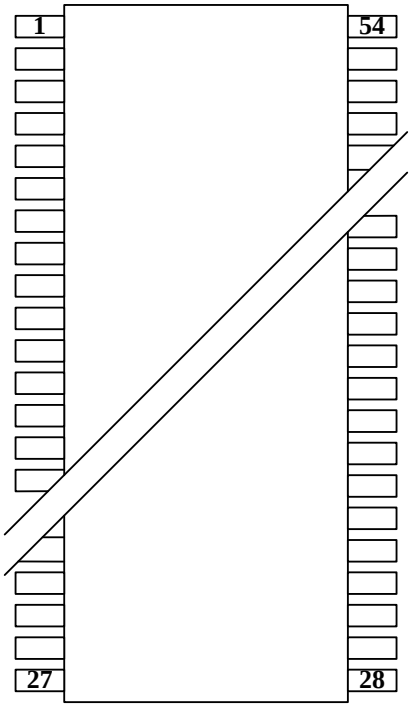

Figure 2 Pin configuration

Table 1 Pin description

Pin	Name	Function
#CS0	Chip select	Disables or enables memory bank1 operation
#CS1	Chip select	Disables or enables memory bank 2 operation
A0 ~ A17	Address	Row/column 18-bit addresses
#WE	Write enable	Enables write operation command to all banks
#OE	Output enable	Enables data output command to all banks
#UB	Upper byte select	Latches upper bytes data(I/O[16:9]) to all banks
#LB	Lower byte select	Latches lower bytes data (I/O[8:1]) to all banks
I/O1 ~ I/O16	Data input/output	Data inputs/outputs 16-bit wide bus.
Vcc/Vss	Power supply/ground	Power and ground for the input/output buffers and core logic.
NC	No connection	This pin is recommended to be left No Connection on the device.

5 Electrical Specifications

5.1 Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Parameter	Symbol	Maximum ratings	Unit
Voltage on V_{CC} supply relative to Vss	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to +Vcc+0.5	V
Power Dissipation	P_D	2	W
Operating Temperature Range	T_{OPR}	-55 to +125	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2 Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	——	V_{CC}+0.5	V
Input low voltage	V_{IL}	-0.3	——	0.8	V

5.3 DC Electrical Characteristics Over The Operating

Table 4 DC characteristics

PARAMETERS	Symbol	TEST CONDITIONS	Min	Max	Unit
Output voltage low level	V_{OL}	V_{cc}=5.5V ， I_{OL} = 1mA	——	0.4	V
Output voltage high level	V_{OH}	V_{cc}=4.5V, I_{OH}= -0.5mA	2.4	——	V

6 Typical Application

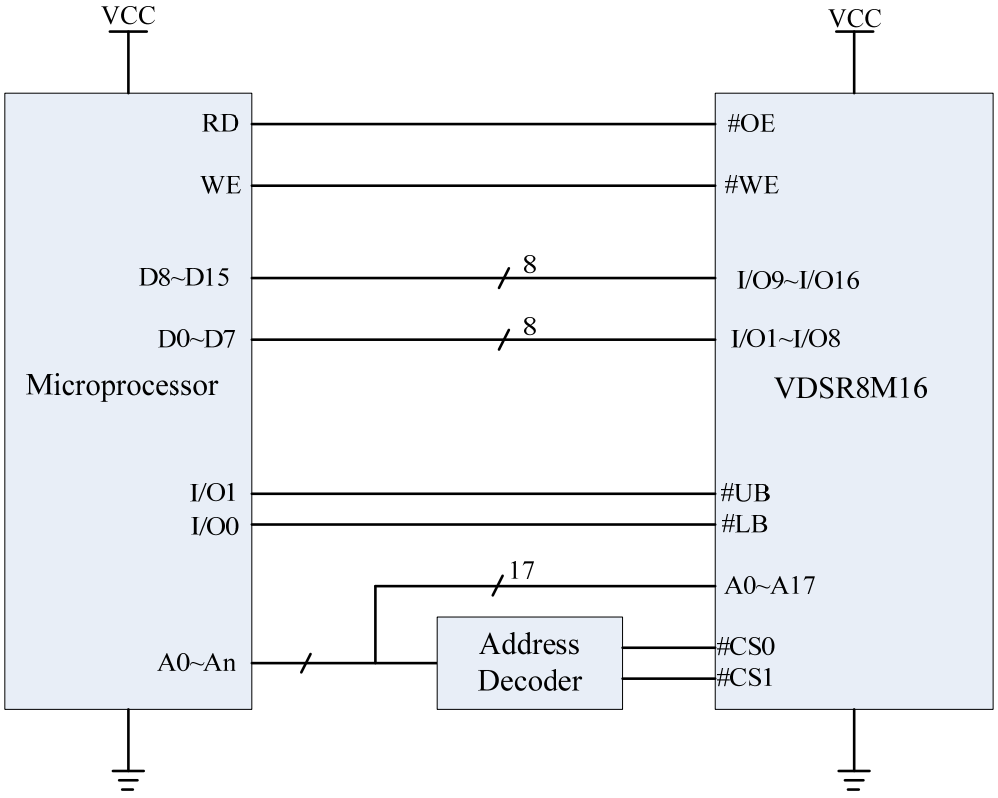

Figure 3 Typical application

7 Ordering Information

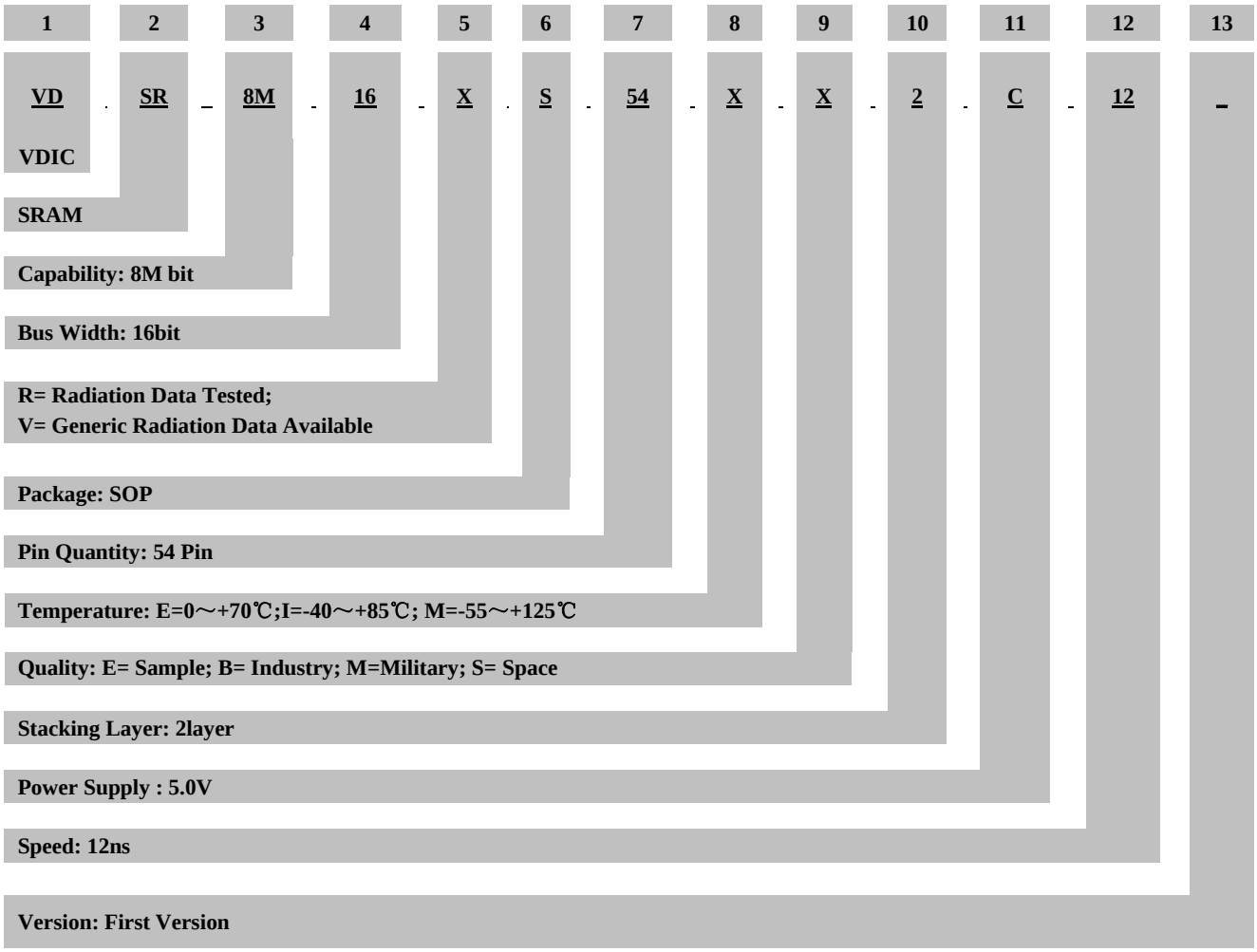

Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VDSR8M16VS54EE2C12	8M	16	-	-	-	SOP54	0 ~ + 70
VDSR8M16VS54IB2C12	8M	16	-	-	-	SOP54	-40 ~ + 85
VDSR8M16VS54MM2C12	8M	16	-	-	-	SOP54	-55 ~ + 125
VDSR8M16RS54MS2C12	8M	16	> 50	> 75	> 2	SOP54	-55 ~ + 125

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8 Package Dimensions

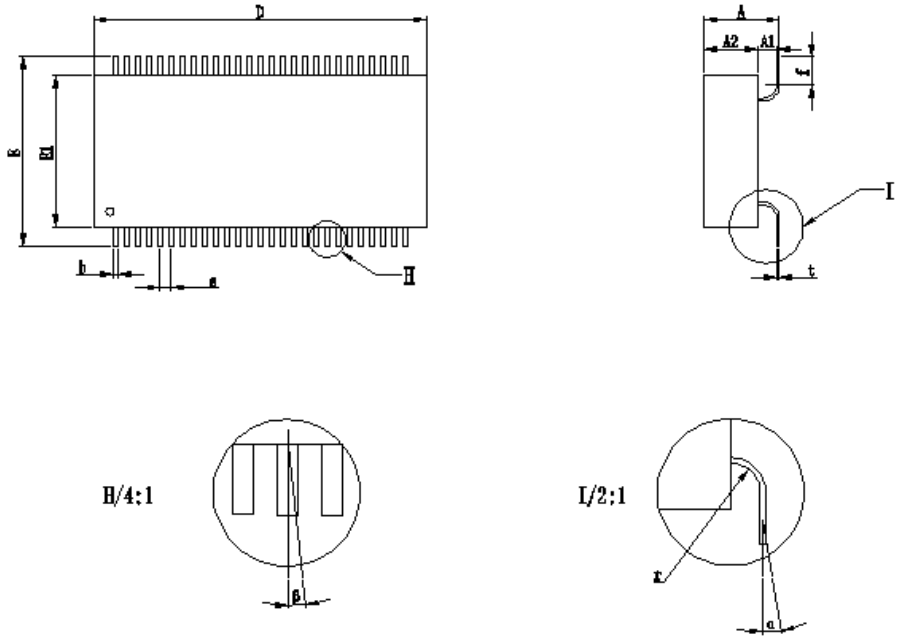

Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	5.40	5.80
A2	3.80	4.40
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35±0.03	
e	0.80	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1. Unit: mm 2. A1= A - A2		

9 REVISION HISTORY

Table 7 Revision history

Revision	Date	Description of Change
A0	Nov 3,2015	First Created
A1	Mar 14,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Add or reduce chapters
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Nov 10,2017	Modified the PACKAGE DIMENSIONS
B0	Oct 18,2018	Revising pin descriptions