VDIC DDR2 SYNCHRONOUS DYNAMIC RAM

VD2D2G16XB95XX2U6 USER MANUAL

Version : A4

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Contents

VDIC-DDR2 SDRAM

HIGH-SPEED 1.8V 128M x 16bit

SYNCHRONOUS DYNAMIC RAM

1. DESCRIPTION

The VD2D2G16XB95XX2U6 is a 2Gbit DDR2 SDRAM high-density System-in-Package memory module.It is organized with 2 chips(with a capacity of 128Mx8).The three-dimensional packaging technology is used to interconnect the multi-layer memory circuits to form a high-density DDR2 memory module with high reliability ,high stability and miniaturization. It is particularly well suited for use in high reliability,high performance and high density system applications,such as servers or workstations.

2. FEATURES

- Organized as 128Mx16
- Power supply:1.8V±0.1V
- SSTL_18 interface
- Clock frequency up to 333MHz
- Programmable CAS Latency: 3,4,5
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5 and 6
- Programmable Burst Length: 4 and 8
- ODT (On-Die Termination)
- Auto Refresh and Self Refresh
- Refresh Interval: 7.8 us (8192 cycles/64 ms)
- Programmable Burst Sequence: Sequential or Interleave
- Package：BGA95
- Available temperature range :

  0℃~+70℃

  -40℃~+85℃

  Specific temperature range can be requested

3. BLOCK DIAGRAM

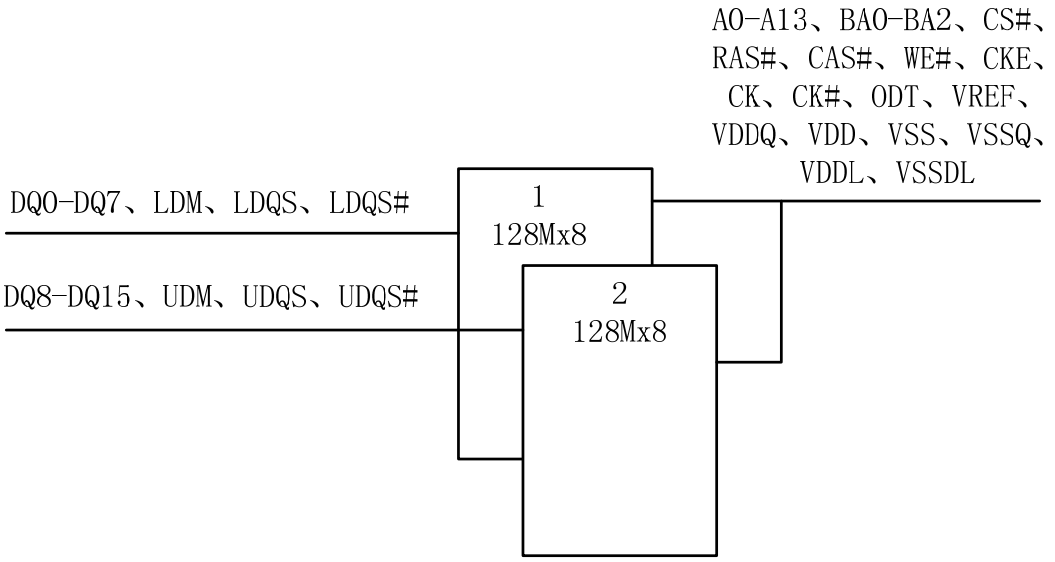


Figure 1 Functional block diagram

4. PIN DESCRIPTIONS

Table 1 Pin Description

PinName	Type	Description
A0-A13	Input	14-bit address inputs. Row Addressing:A0-A13;Column Addressing:A0-A9;Precharge Addressing:A10
RFU/A14	Input	Reserved for future use,as an NC pin inside thememory module.
BA0-BA2	Input	3-bit Bank Address inputs.
CAS#	Input	CAS# Command input.
RAS#	Input	RAS# Command input.
WE#	Input	WE# Command input.
ODT	Input	On Die Termination Enable input.
CK,CK#	Input	Differential clock inputs.
CKE	Input	Clock Enable input.
LDM,UDM	Input	Data Mask input.LDM for DQ0-DQ7;UDM for DQ8-DQ15.
LDQS,LDQS#,UDQS,UDQS#	Input/Output	Data Strobe(Differential signals):output with read data,input with write data.LDQS,LDQS# for DQ0-DQ7;UDQS,UDQS# for DQ8-DQ15.
DQ0-DQ15	Input/Output	Data Input/Output.
VDD	Supply	Power supply.
VSS	Supply	Ground.
VDDQ	Supply	DQ power supply.
VSSQ	Supply	DQ ground.
VDDL	Supply	DLL power supply.
VSSDL	Supply	DLL ground.
VREF	Supply	Reference voltage.

5. PIN ASSIGNMENT

	1	2	3	4	5	6	7	8
A		VDD	DQ9	VSSQ	VSSQ	LDQS	LDQS#	VDDQ
B	DQ6	DQ1	LDM	UDM	UDQS	UDQS#	DQ7	VSSQ
C	VSSQ	DQ14	DQ3	VDDQ	VDDQ	DQ8	DQ15	DQ0
D	VDDQ	DQ11	VDDQ	VSSQ	VSSQ	VDDQ	DQ2	VSSQ
E	VSSQ	DQ12	DQ4	VSSQ	VSSQ	DQ5	DQ10	VDDQ
F	VREF	VDDQ	VDDL	VSSQ	VSSQ	VSSDL	DQ13	VSSQ
G	VDD	WE#	CKE	VSS	VSS	ODT	CK	VSS
H	VSS	BA1	BA2	VSS	VSS	RAS#	CK#	VDD
J	VDD	BA0	VSS	VSS	VSS	CAS#	CS#	VSS
K	VSS	A1	A10	VSS	VSS	VDD	A0	VDD
L	A3	A7	RFU/A14	VDD	A11	A13	A4	A2
M	VSS	A12	A9	A5	A6	VSS	A8	VSS

TOP VIEW

Figure 2 Pin assignment

6. DC OPERATING CONDITIONS

6.1. ABSOLUTE MAXIMUM DC RATINGS

Table 2 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on VDD pin relative to VSS	VDD	-1.0 ~ 2.3	V
Voltage on VDDQ pin relative to VSS	VDDQ	-0.5~2.3	V
Voltage on VDDL pin relative to VSS	VDDL	-0.5~2.3	V
Voltage on any pin relative to VSS	V_{IN}, V_{OUT}	-0.5~ 2.3	V
Input Leakage Current	V_I	-5~5	uA
Output Leakage Current	I_{OZ}	-5~5	uA
VREF Leakage Current	I_{VREF}	-2~2	uA
Power dissipation	P_{DMAX}	1	W
Storage temperature	T_{STG}	-55 ~ +150	°C

6.2. Recommended DC Operating Conditions (SSTL_1.8)

Table 3 Recommended DC Operating Conditions

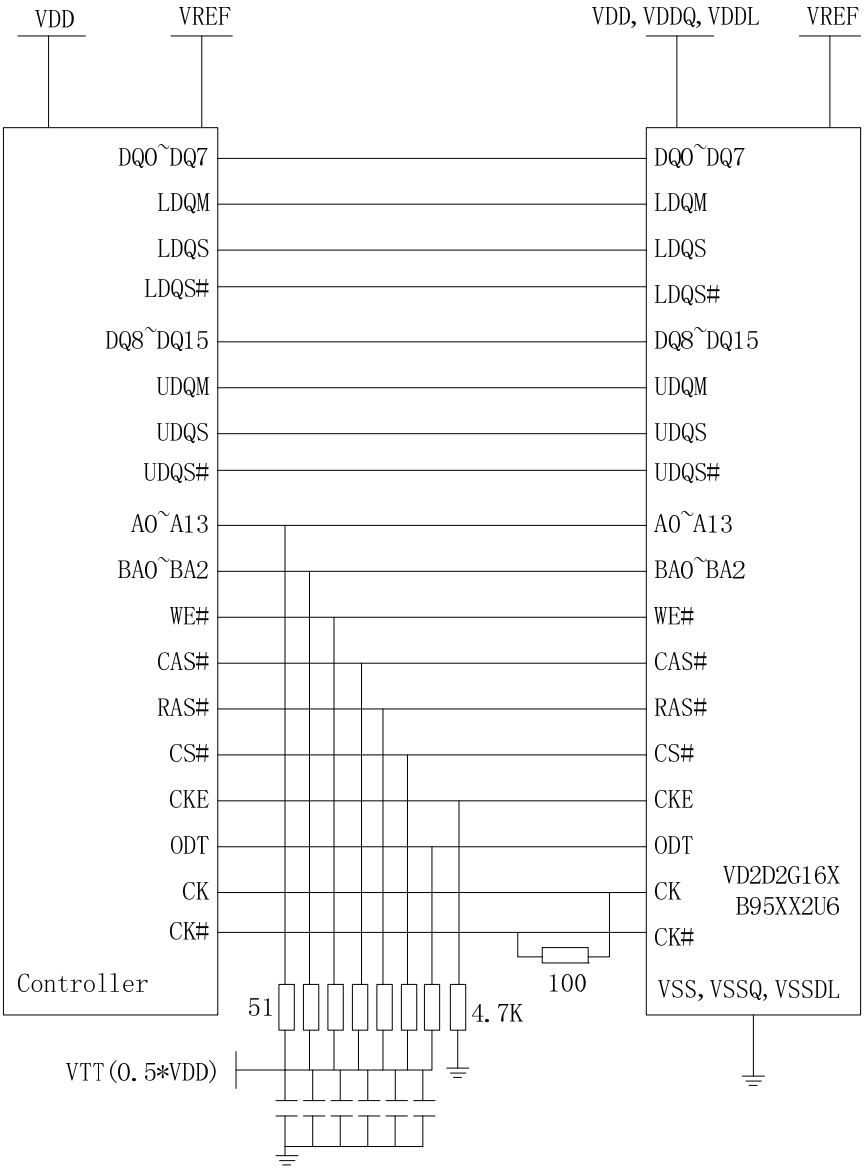
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.7	1.8	1.9	V
Supply Voltage for DLL	VDDL	1.7	1.8	1.9	V
Supply Voltage for Output	VDDQ	1.7	1.8	1.9	V
Input Reference Voltage	VREF	0.49*VDDQ	0.5*VDDQ	0.51*VDDQ	V
Clock Frequency	f			333	MHz

6.3. DC Characteristics

Table 4 DC Characteristics

Parameter	Symbol	Value	Unit
Operating Current(One bank active)	IDD1	230	mA
Precharge power-down standby current	IDD2P0	30	mA
Active power-down current	IDD3P	30	mA

7. TYPICAL APPLICATION



Note:
1. Termination resistor needs to placed close to the DDR2 device.
2. For ADDR/CMD/CTRL VTT termination, every four termination resistors should be accompanied by one 1.0uF capacitor, physically interleaving among resistors.

Figure 3 Typical application

8. ORDERING INFORMATION

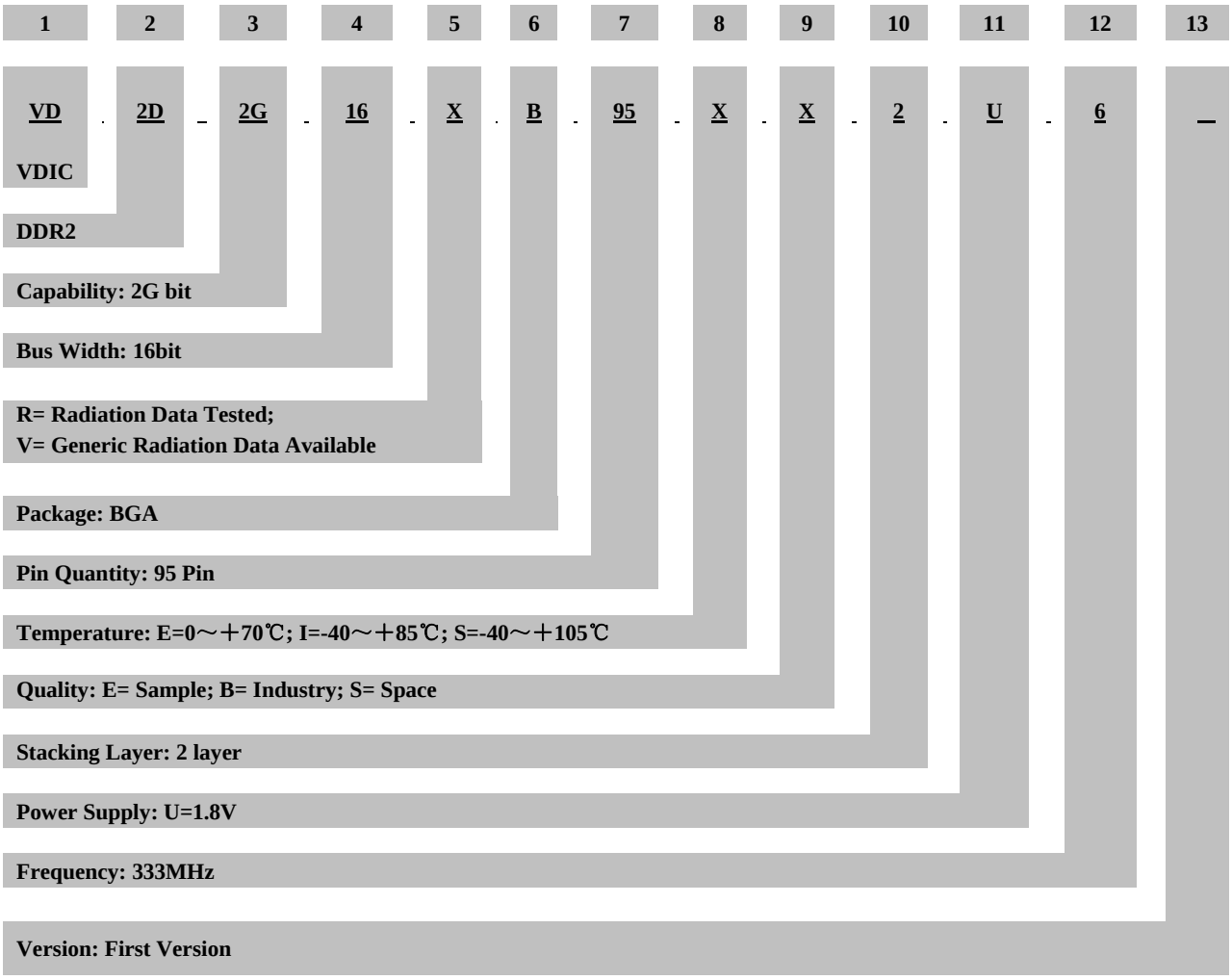


Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VD2D2G16VB95EE2U6	2G	16	-	-	-	BGA95	0 ~ +70
VD2D2G16VB95IB2U6	2G	16	-	-	-	BGA95	-40 ~ +85
VD2D2G16RB95SS2U6	2G	16	150	TBD	TBD	BGA95	-40 ~ +105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

9. PACKAGE DIMENSIONS

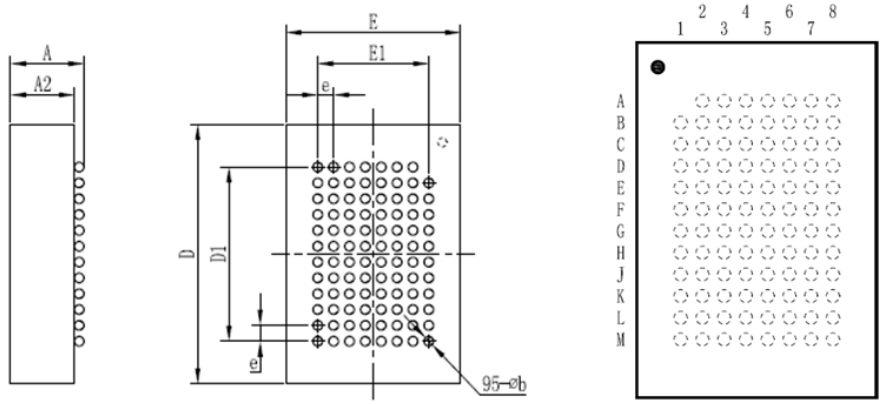


Figure 4 Package dimensions

	Min	Max
A	5.60	6.20
A2	4.80	5.40
D	20.60	21.00
D1	13.97	
E	13.80	14.20
E1	8.89	
b	0.76	
e	1.27	
NOTE: 1.Unit: mm 2. A1= A - A2		

10.REVISION HISTORY

Table 6 Revision history

Revision	Date	Description of Change
A0	Sep 28, 2018	First Created
A1	DEC 24, 2019	Part Number modified
A3	Mar.,2020	Update TID and SEE
A4	Jun., 2020	Modify the content