VDIC DDR1 SYNCHRONOUS DYNAMIC RAM

VD1D8G08XS66XX8T7B-Ⅱ USER MANUAL

Version :B0

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Contents

VDIC-DDR SDRAM

HIGH-SPEED 2.5V 1G x 8bit

SYNCHRONOUS DYNAMIC RAM

1. DESCRIPTION

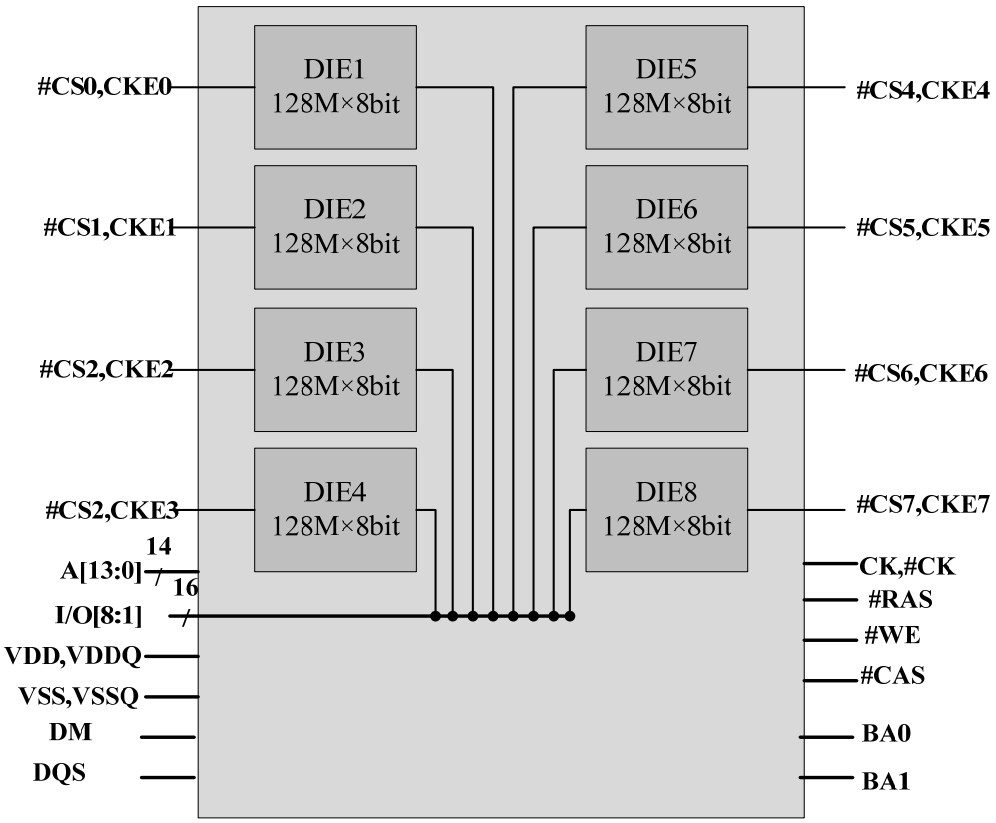
The VD1D8G08XS66XX8T7B-Ⅱ is a 8192M bits DDR1 SDRAM, organized as 1G words× 8 bits. The device has eight dies, each die includes 1Gbit. The device has a 8-bit interface and is selected with specific #CS,#CK and CKE. The device is useful for a variety of high bandwidth, high performance memory system applications. It is packaged in standard 66-pin SOP.

2. FEATURES

- Stack of eight 1Gbit DDR SDRAM.
- Organized as 1Gx8-bit.
- Power supply: V_{DD}, V_{DDQ}=2.5V±0.2V.
- Double-data-rate architecture; two data transfer per clock cycle.
- Internal pipelined operation; column address can be changed every clock cycle.
- Bidirectional data strobe.
- Differential clock inputs (CK AND #CK).
- DLL aligns DQ and DQS transition with CK transition,.
- Programmable Read Latency 2, 2.5(clock).
- Programmable Burst length (2, 4, 8).
- Programmable Burst type (sequential & interleave).
- Edge aligned data output, center aligned data input.
- Auto & Self refresh, 7.8μs refresh interval (8192/64ms refresh).

3. BLOCK DIAGRAM

Figure 1:Block Diagram



(All other signals are common to the eight memories)

Figure 1 Block diagram

4. PIN DESCRIPTIONS

Figure 3: Pin Descriptions

Pin Id	Pin #		Pin Id
VDD	1	66	VSS
DQ0	2	65	DQ7
VDDQ	3	64	VSSQ
CKE6	4	63	CKE1
DQ1	5	62	DQ6
VSSQ	6	61	VDDQ
#CS1	7	60	CKE2
DQ2	8	59	DQ5
VDDQ	9	58	VSSQ
#CS2	10	57	CKE3
DQ3	11	56	DQ4
VSSQ	12	55	VDDQ
#CS3	13	54	CKE4
#CS4	14	53	CKE5
VDDQ	15	52	VSSQ
#CS5	16	51	DQS
A13	17	50	DNU
VDD	18	49	VREF
DNU	19	48	VSS
#CS6	20	47	DM
#WE	21	46	#CK
#CAS	22	45	CK
#RAS	23	44	CKE0
#CS0	24	43	CKE7
#CS7	25	42	A12
BA0	26	41	A11
BA1	27	40	A9
AP/A10	28	39	A8
A0	29	38	A7
A1	30	37	A6
A2	31	36	A5
A3	32	35	A4
VDD	33	34	VSS

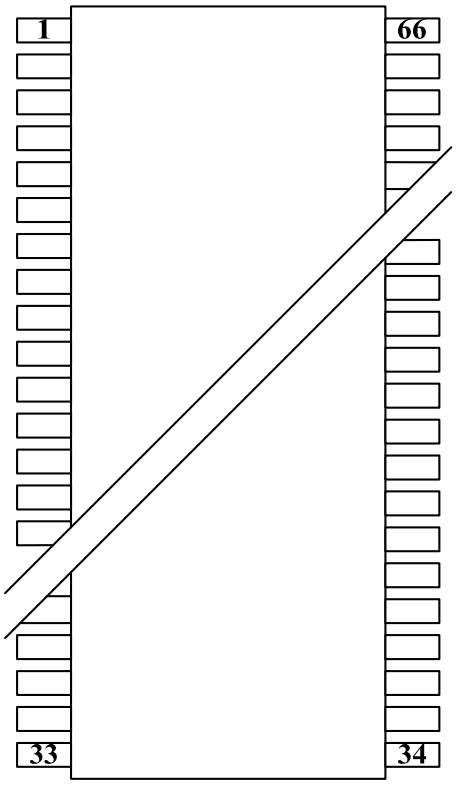


Figure 2 Pin configuration

Table 1 Pin description

Name	Function
A0~A13	Address Input. Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA0, BA1) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER (LMR) command.
DQ0-DQ7	Data Input/Output Ports. 8bi-directional ports are used to read data from, or write data into the DDR1 SDRAM.
#CS0-#CS7	Die Enable Input. When #CS is Low, the command input cycle becomes valid. When CSn is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.
BA0,BA1	Bank address inputs: BA0 and BA1 define the bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also define which mode register (mode register or extended mode register) is loaded during the LOAD MODE REGISTER command.
#RAS	Row address strobe. Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
#CAS	Column address strobe. Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
#WE	Write Enable Input. Enables write operation and row precharge. Latches data in starting from CAS, #WE active.
DM	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
DQS	Data strobe: Output with read data, input with write data. DQS is edge-aligned with read data, center-aligned with write data. It is used to capture data.
CK,CK#	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of #CK. Output data (DQ and DQS) is referenced to the crossings of CK and #CK.
CKE	Clock enable: CKE HIGH activates and CKE LOW deactivates the internal clock, input buffers, and output drivers. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle) or ACTIVE power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit and for disabling the outputs. CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK, #CK, and CKE) are disabled during power-down. Input buffers (excluding CKE) are disabled during SELF REFRESH. CKE is an SSTL_2 input but will detect an LVCMOS LOW level after V_{DD} is applied and until CKE is first brought HIGH, after which it becomes a SSTL_2 input only.
V_{DD},V_{DDQ}	Power supply, connect to 2.5V
V_{REF}	SSTL_2 reference voltage.

Name	Function
V_{SS},V_{SSQ}	Ground
NC,DNU	No connect

5. ELECTRICAL SPECIFICATIONS – DC and AC

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.1. Absolute Maximum Ratings

Table 2 Absolute maximum ratings

Characteristics	Symbol	Maxinmum ratings	Unit
Voltage on V_{DD} supply relative to Vss	V_{DD}/ V_{DDQ}	-1 ~ 3.6	V
Voltage on any pin relative to Vss	V_{IN}	-0.5 to V_{DDQ}+0.5	V
Power Dissipation	P_D	2.0	W
Operating Temperature Range	T_{OPR}	-55~ +105	℃
Storage Temperature Range	T_{STG}	-65 to +150	℃

5.2. Recommended DC Operating Conditions

Table 3 Recommended DC operating condition

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	2.3	2.5	2.7	V
I/O Supply Voltage	V_{DDQ}	2.3	2.5	2.7	V
I/O Reference Voltage	V_{REF}	0.49×V_{DDQ}	—	0.51×V_{DDQ}	V
I/O Termination Voltage(System)	V_{TT}	V_{REF}-0.04	—	V_{REF}+0.04	V
Input high Voltage	$V_{IH(DC)}$	V_{REF}+0.15	—	V_{DD}+0.3	V
Input Low Voltage	$V_{IL(DC)}$	-0.3	—	V_{REF}-0.15	V

5.3. DC Electrical Characteristics and Operating Conditions

Table 4 DC characteristics

Technical Parameters	symbol	Test Conditions	Min	Max	Uint
Input leakage current low /high	I_{LIL}	V_{DD}=2.7V，V_{REF}=1.35V, V_{in}=0V	-2	2	μA
	I_{LIH}	V_{DD}=2.7V，V_{REF}=1.35V V_{in}=V_{DDQ}	-2	2	μA
Output leakage current low/high	I_{LOL}	V_{DD}=2.7V，V_{REF}=1.35V，V_{out}=0V	-5	5	μA
	I_{LOH}	V_{DD}=2.7V，V_{REF}=1.35V ， V_{out} =V_{DDQ}	-5	5	μA

6. TYPICAL APPLICATION

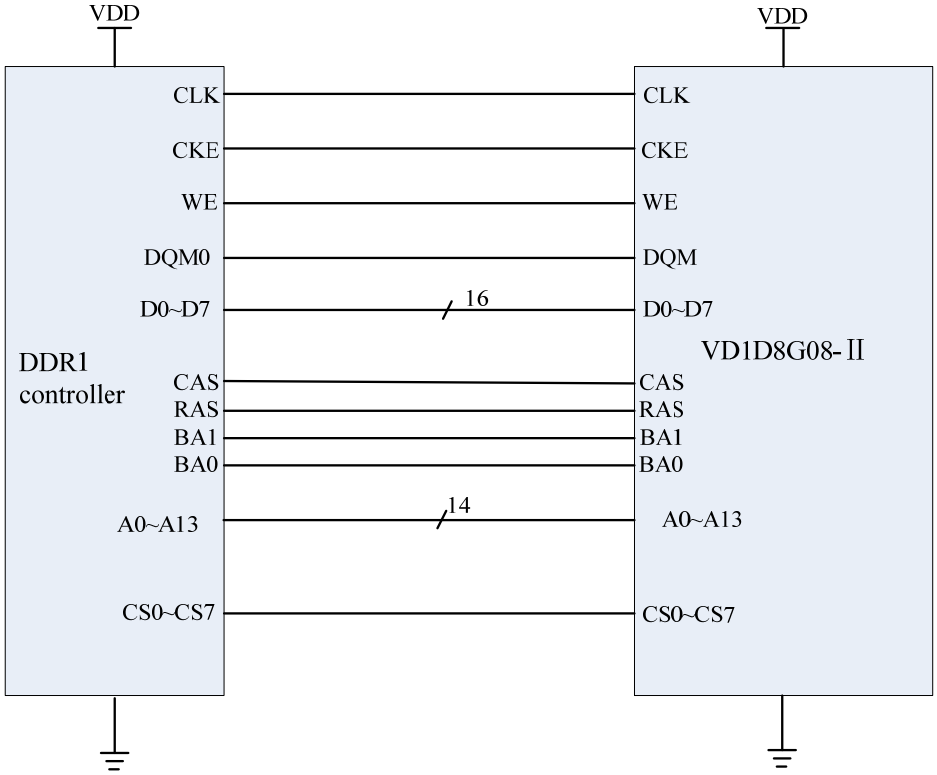


Figure 3 Typical application

7. ORDERING INFORMATION

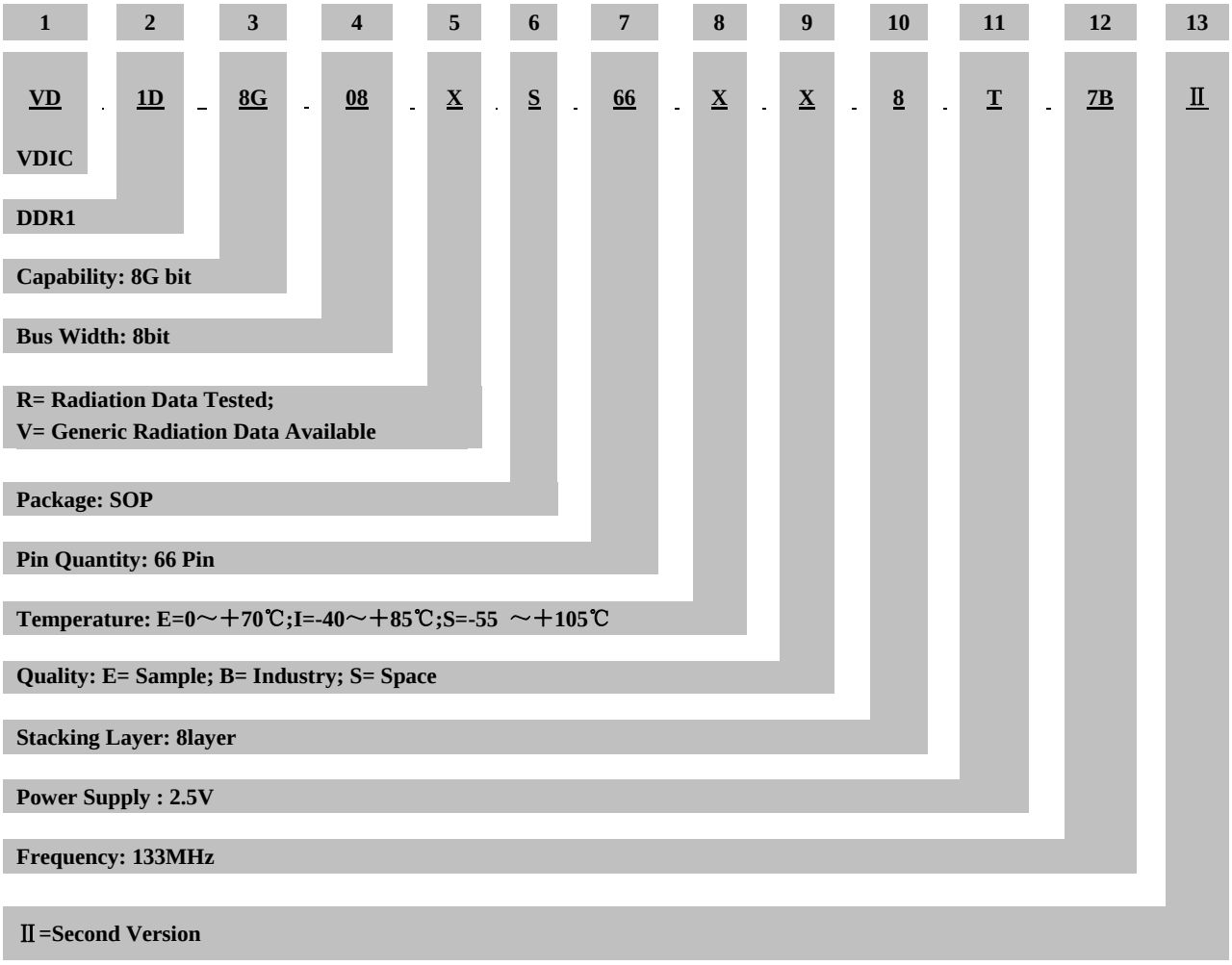


Table 5 Ordering information

Part Number	Capacity (bit)	Bus Width (bit)	Radiation			Packaging	Temperature (℃)
			TID[1]	SEL[2]	SEU[3]		
VD1D8G08VS66EE8T7B-Ⅱ	8G	08	-	-	-	SOP66	0 ~ + 70
VD1D8G08VS66IB8T7B-Ⅱ	8G	08	-	-	-	SOP66	-40 ~ + 85
VD1D8G08RS66SS8T7B-Ⅱ	8G	08	TBD	TBD	TBD	SOP66	-55 ~ + 105

[1] TID: Total Dose（Krads(Si)）
[2] SEL: LET Threshold（Mev.cm2/mg）
[3] SEU:SEU Threshold （Mev.cm2/mg）

8. PACKAGE DIMENSIONS

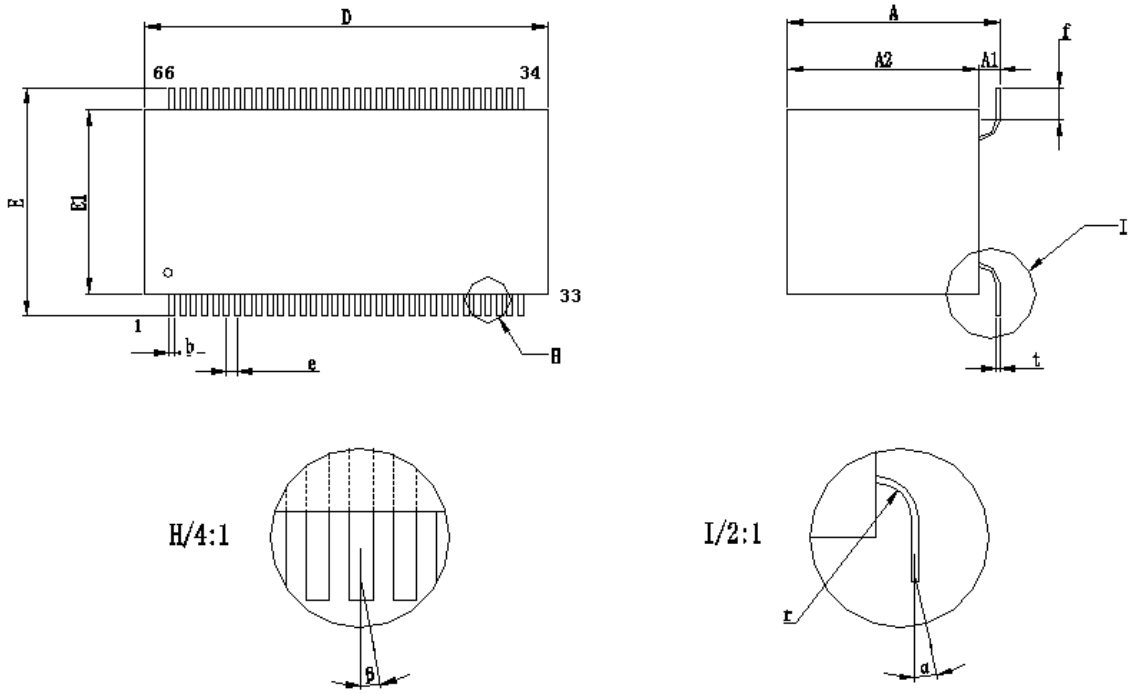


Figure 4 Package dimensions

Table 6 Dimensions information

	Min	Max
A	12.30	12.80
A2	11.10	11.50
D	23.80	24.20
E	13.40	13.80
E1	10.80	11.20
f	2.00	
b	0.35	
e	0.65	
r	1.00	
t	0.20	
α	≤3°	
β	≤3°	
NOTE: 1.Unit: mm 2. A1= A - A2		

9. REVISION HISTORY

Table 7 Revision historys

Revision	Date	Description of Change
A0	Nov 5,2015	First Created
A1	Mar 21,2016	Modified the PIN DESCRIPTIONS
A2	Aug 23,2016	Modified the ORDERING INFORMATION
A3	Jan 9,2017	Modified the Package dimensions figure.
A4	Oct.25,2017	Changed company's name to Zhuhai Orbita Aerospace Science & Technology Co.，Ltd
A5	Mar 15,2018	Add or reduce the chapters.
B0	Mar 23,2020	Update TID and SEE